THE ART AND SCIENCE of PCB DESIGN

lecture 3- LAYOUT ! OMG !

We have circuit in schematic! **Now we want to** *put that circuit on a board*

while considering parasitics, manufacturing, and signal integrity!

Follow these guys on instagram @mit_solar_car

ANNOUNCEMENT - END OF IAP DANCY PARTY!!!

(This class is about Art + Science, so we can't justttt do something intellectual to celebrate the fact that you can design PCBS! We need to include art!)

(So we're having a dance party - w/ food ofc)

Wed, Feb 1st, 7-9 PM! @ Lobby 13

(Yes, you can invite your friends!)

OUTLINE

- what is layout / Electron herding / steps to layout
- Placing components
- Tools for connection
- Layout considerations
- CASE STUDIES ON GOOD LAYOUT!!!

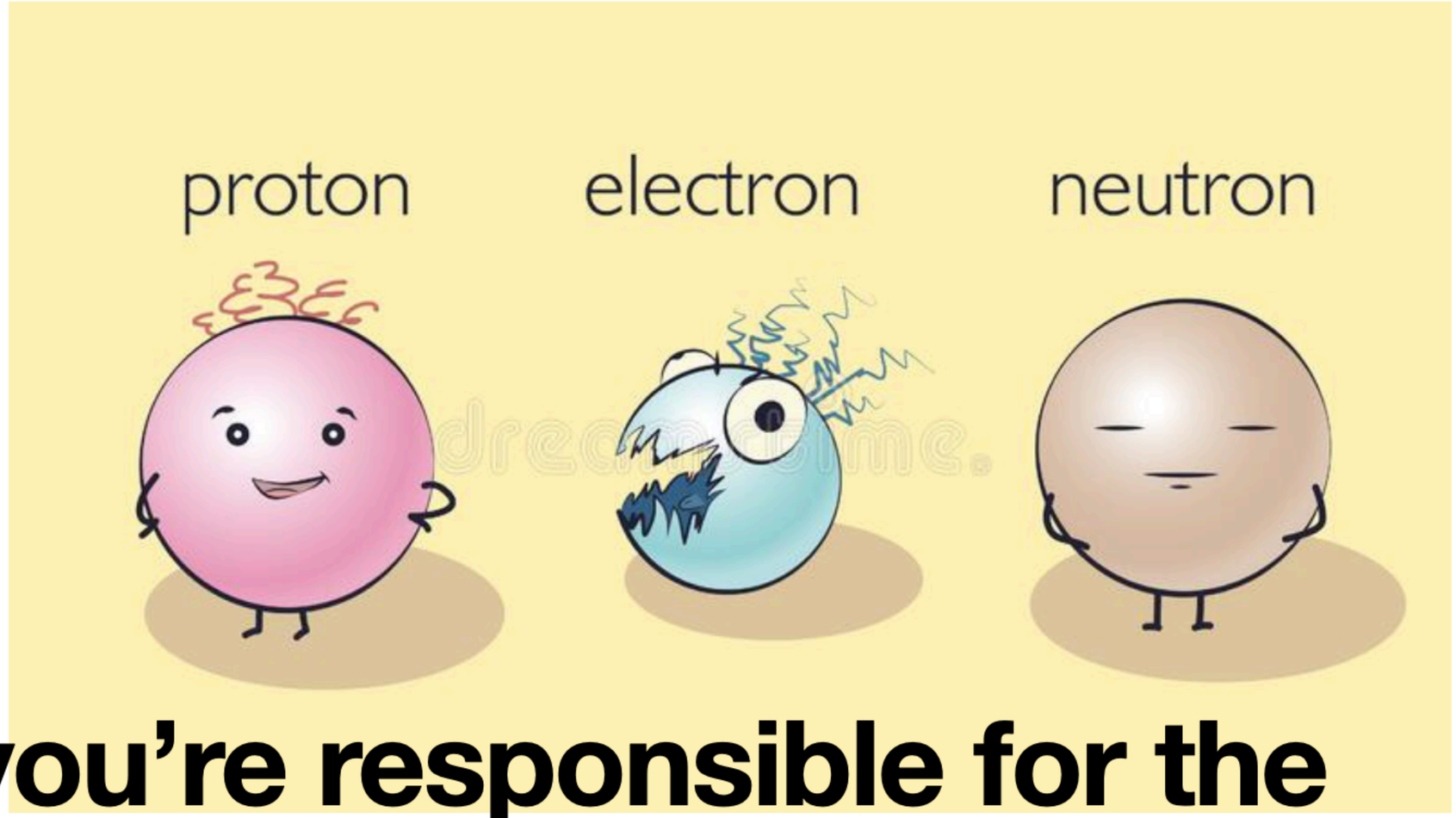
(Introduction to urban planning for the distinguished electrical engineer)

Layout is the FUN PART!

(This is where the ART comes in, a good layout is like a beautiful little metropolis of electrons)

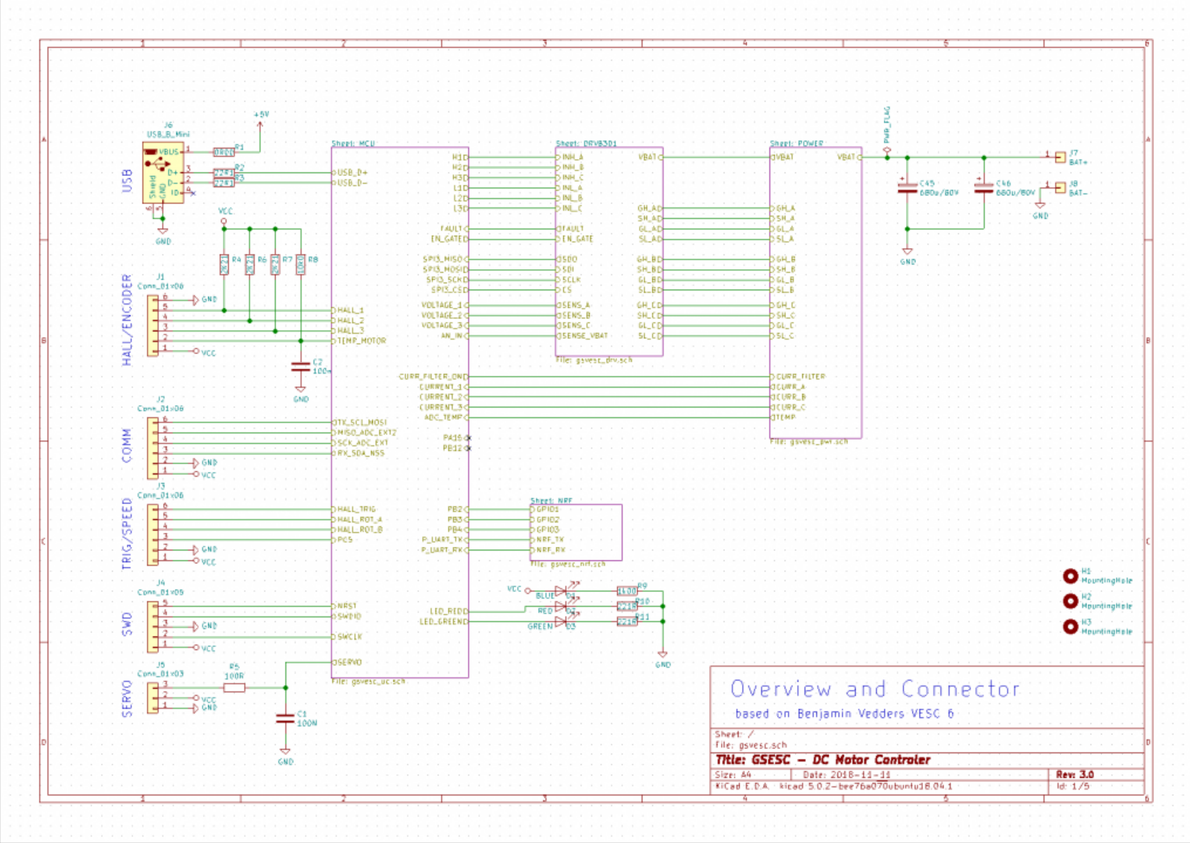
(You herd these electrons where they need to go using layout)

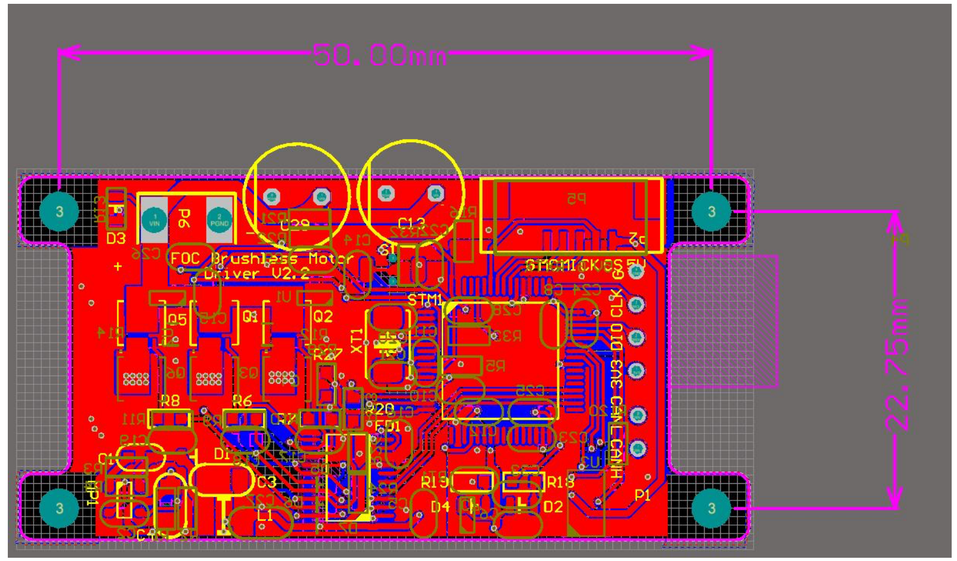
Get ready.



^ you're responsible for the child in the middle

vesc-project.com



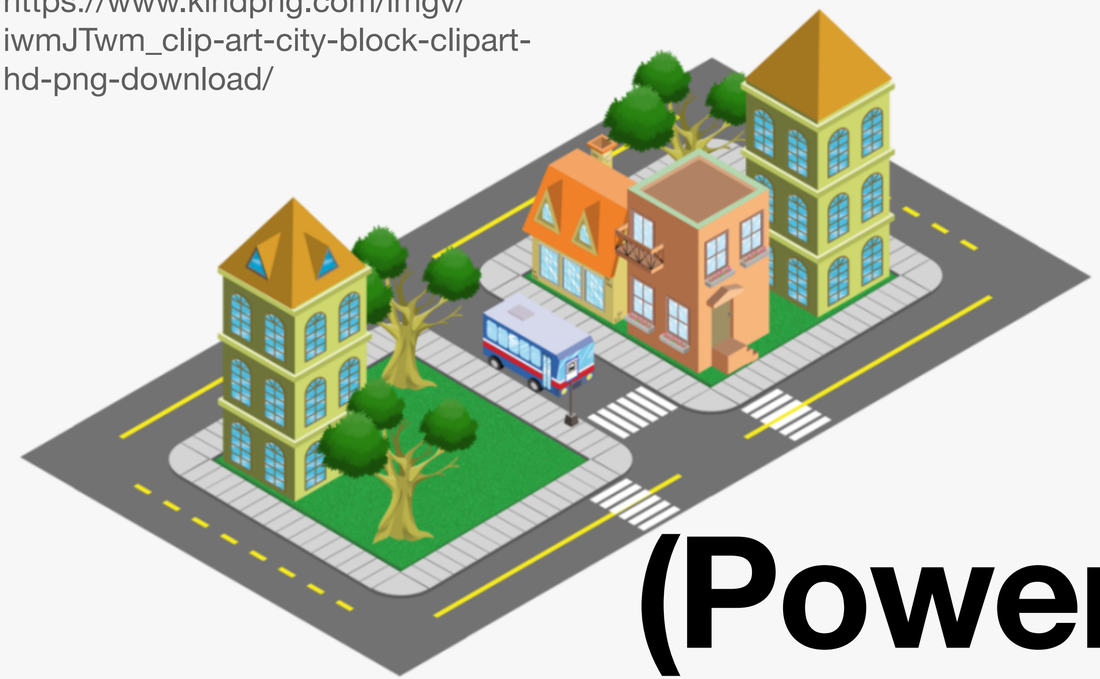


(This is where we connect everything yes, but it's also where we consider all the un-ideal things that happen in the real world and how we can fix them with design)

Components on the board, placement & orientation!

Separation of Power + Signal.

https://www.kindpng.com/imgv/iwmJTwm_clip-art-city-block-clipart-hd-png-download/



(Power block)

https://www.dreamstime.com/illustration/isometric-city-blocks-concept.html

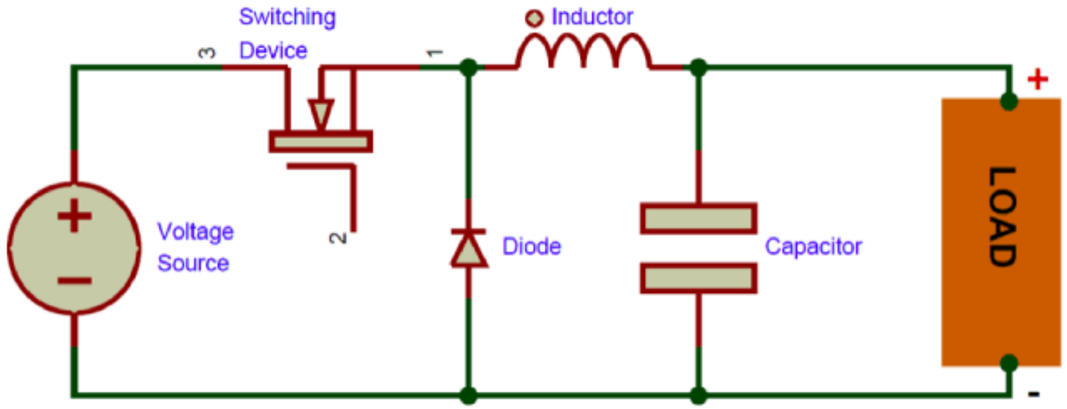
(Signal block)

@ MIT

Tell me whyyy??

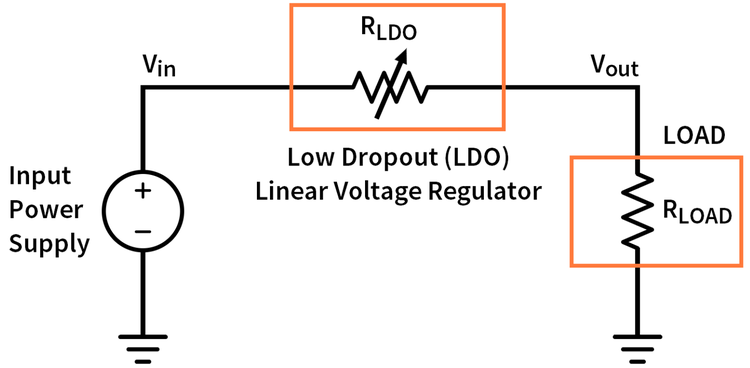
(Ain’t nothing but a partttyyyyyy…)

Power, LDOs, Switching Converters, Digital, Analog



https://components101.com/articles/buck-converter-basics-working-design-and-operation

(Put these far from sensitive electronics, switching produces noise!)

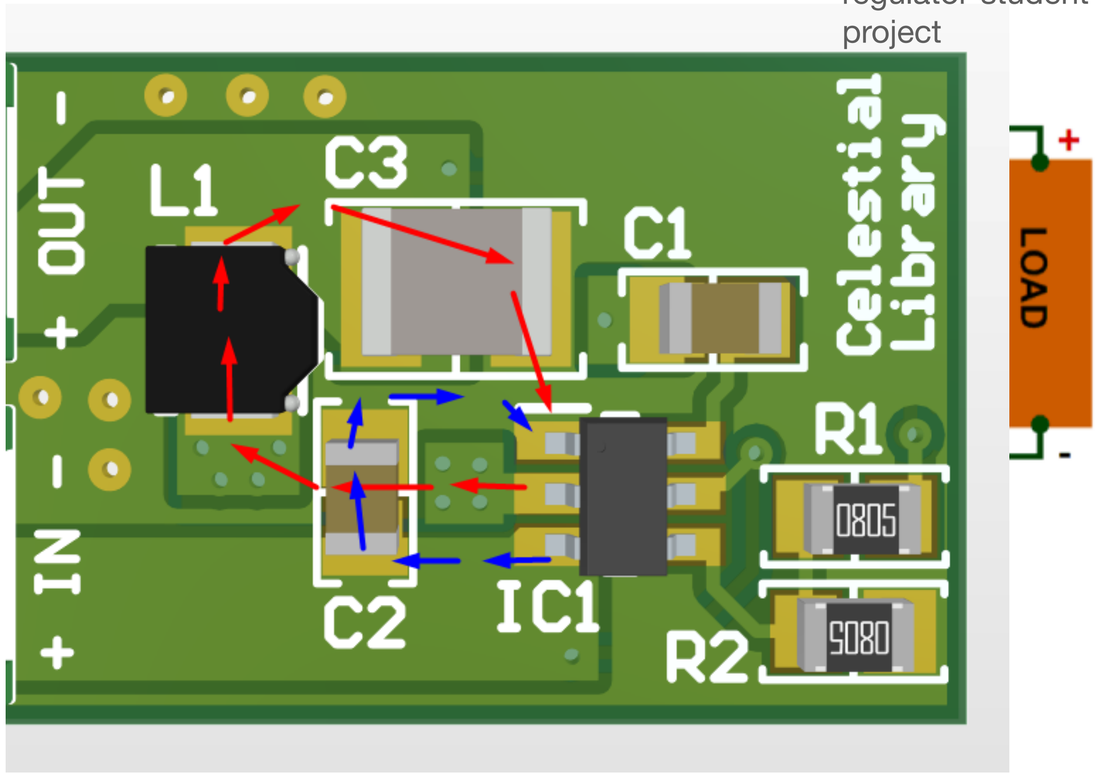


https://www.circuitbread.com/ee-faq/when-should-you-choose-ldo-or-buck-converter

(Put these NEAR chips, because they SMOOTH the voltage signal, small trace so less time to pick up noise)

Power, LDOs, Switching Converters, Digital, Analog

https://resources.altium.com/p/build-dc-dc-buck-regulator-student-project



https://sg.rs-online.com/web/p/voltage-regulators/9210603

(As tightly packaged as possible)

(Put these NEAR chips, because they SMOOTH the voltage signal, small trace so less time to pick up noise)

Separation of Power + Signal.

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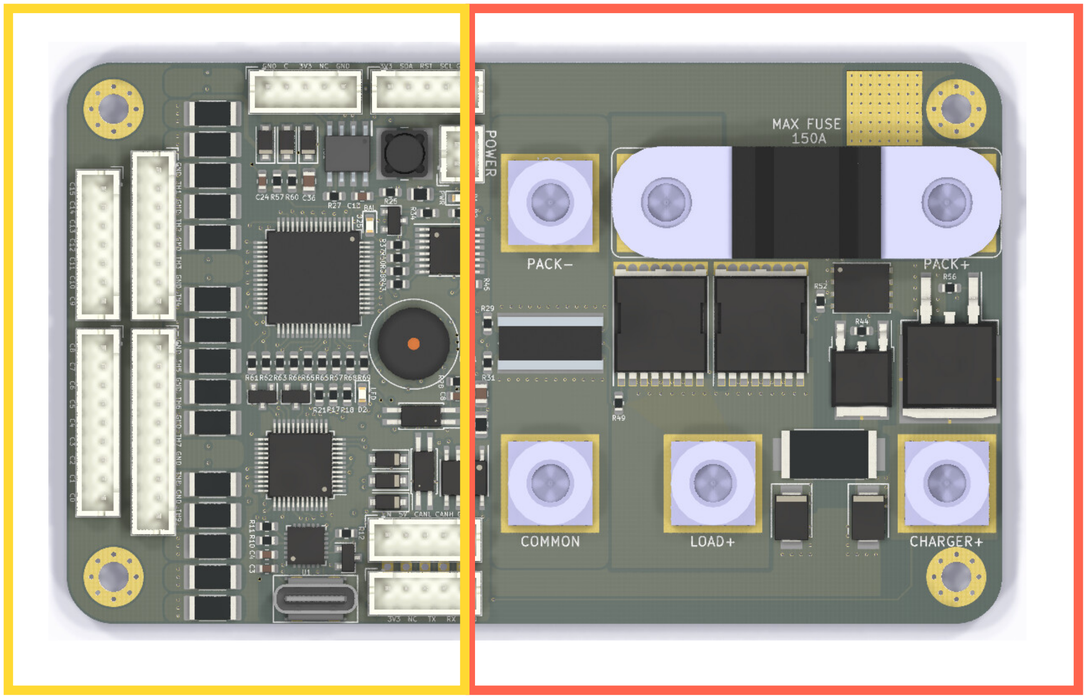
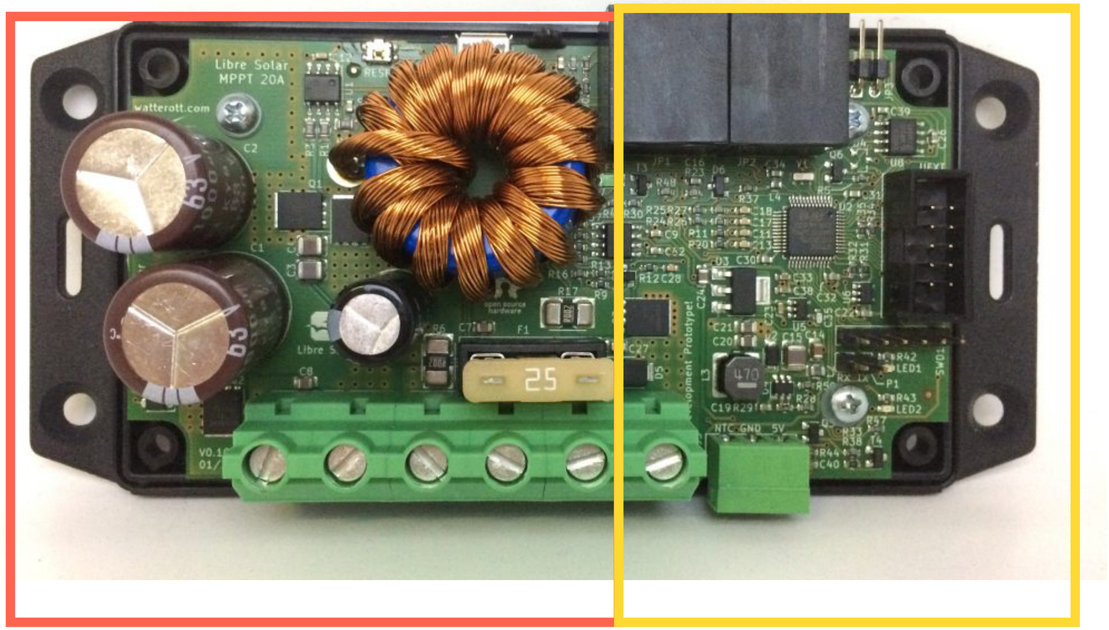


Signal

Power

https://forum.esk8.news/t/diebiems-fork-ennoid-bms-for-6s-to-24s-battery-packs/45490?page=6

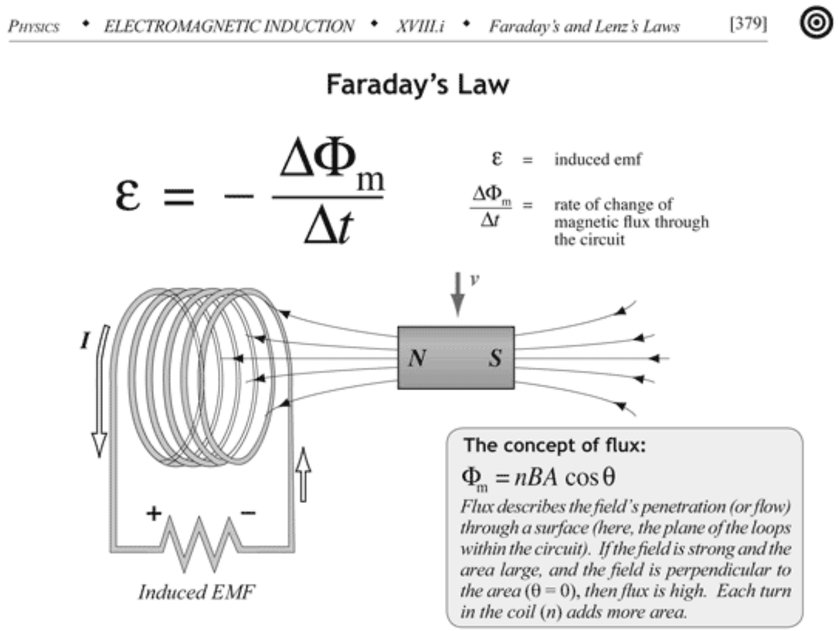
https://www.fablab-hamburg.org/the-libre-solar-project/



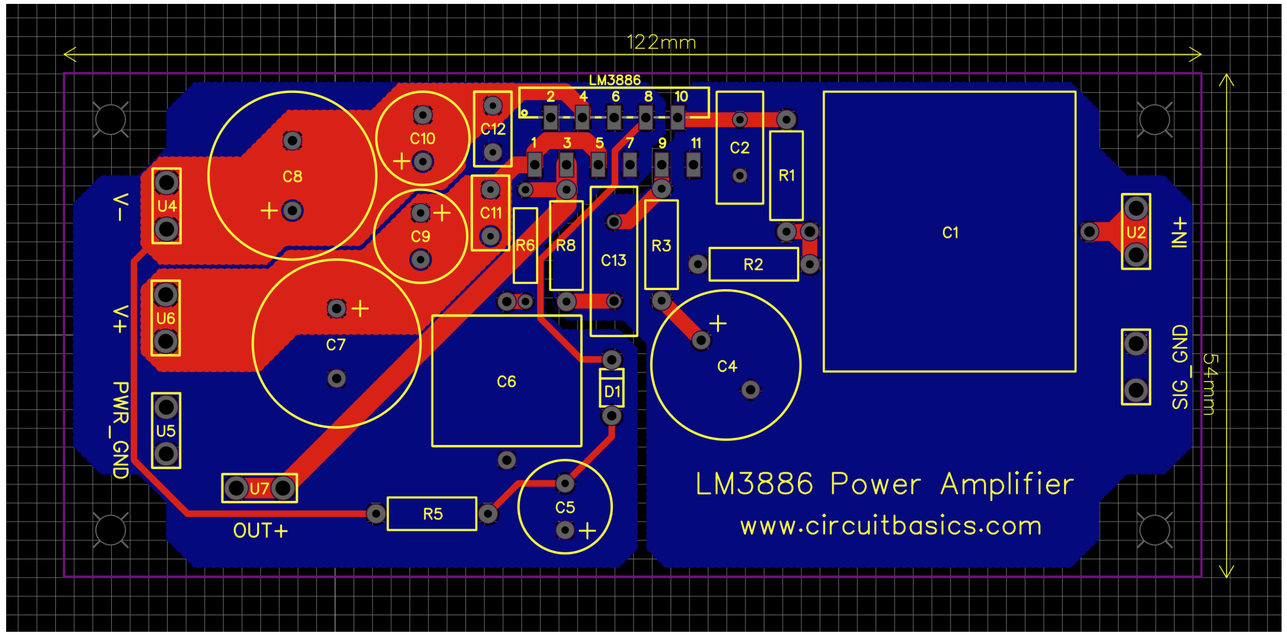
Power

Signal

Orientation + Minimization of Trace Length, Inductance Loops.

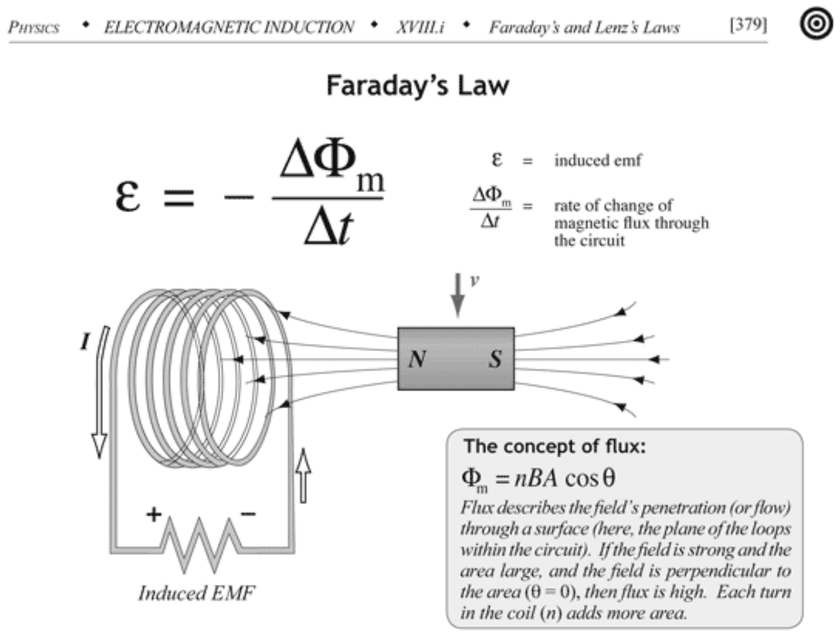


https://sites.suffolk.edu/kdshepard/2013/03/07/faradays-law/

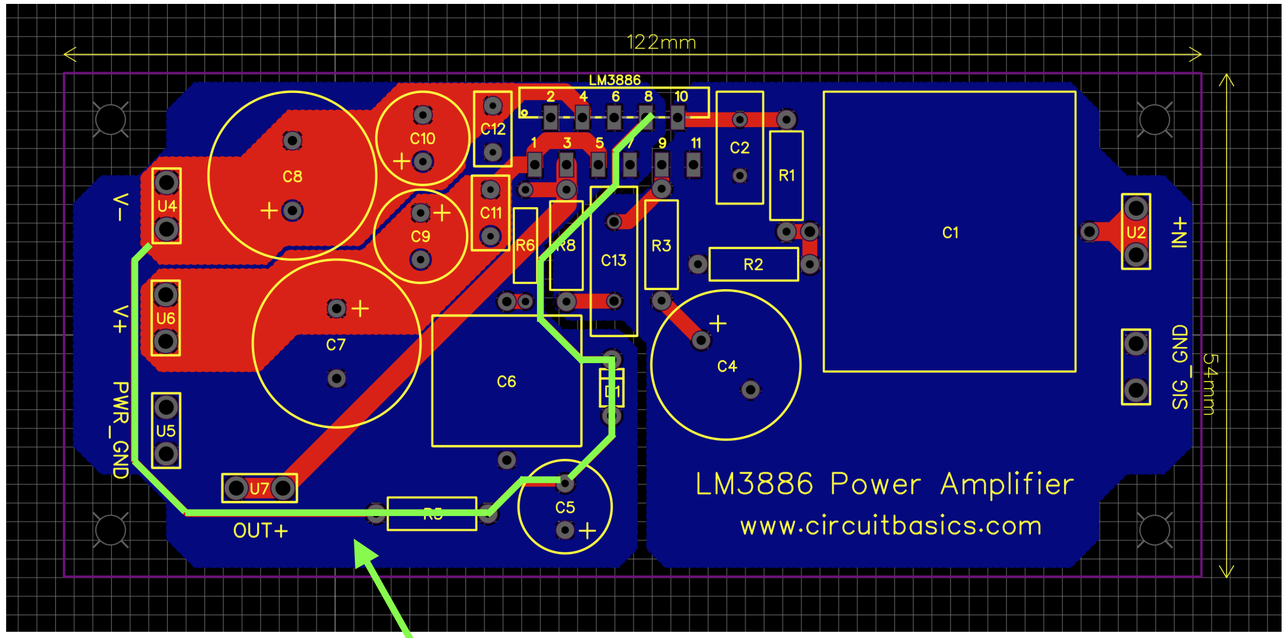


https://www.circuitbasics.com/what-is-pcb-design/

Orientation + Minimization of Trace Length, Inductance Loops.



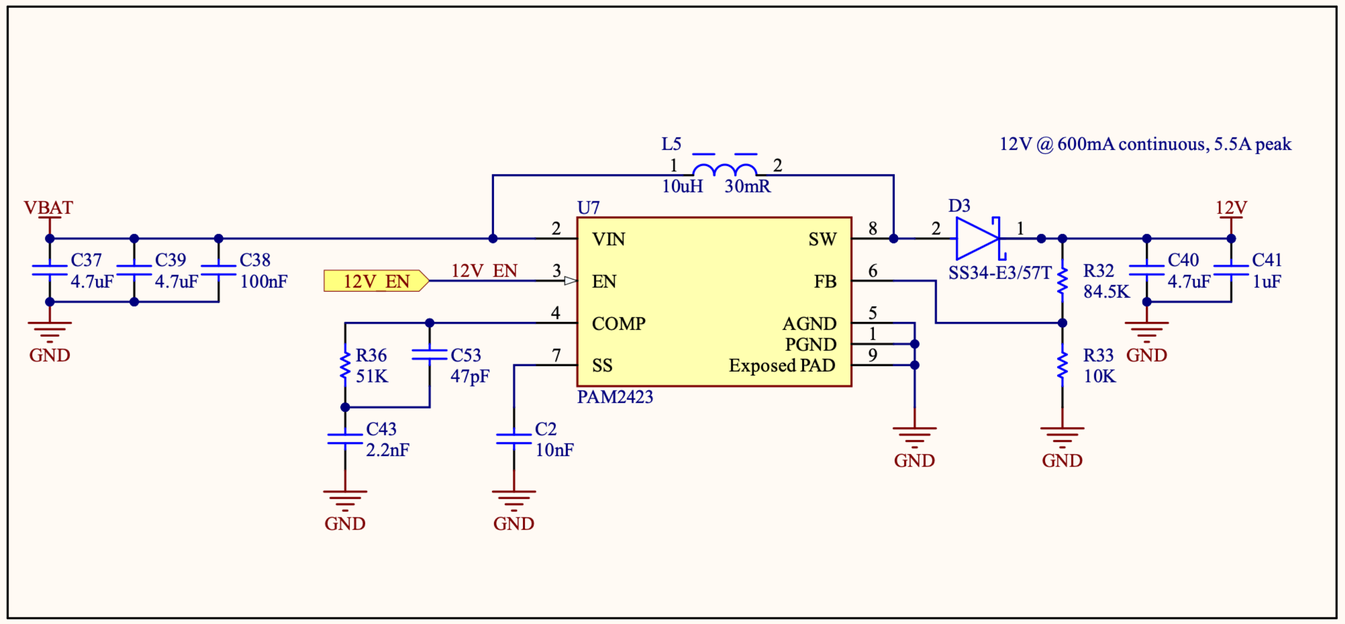
https://sites.suffolk.edu/kdshepard/2013/03/07/faradays-law/



https://www.circuitbasics.com/what-is-pcb-design/

Very Large Loop = Bad, especially near power components

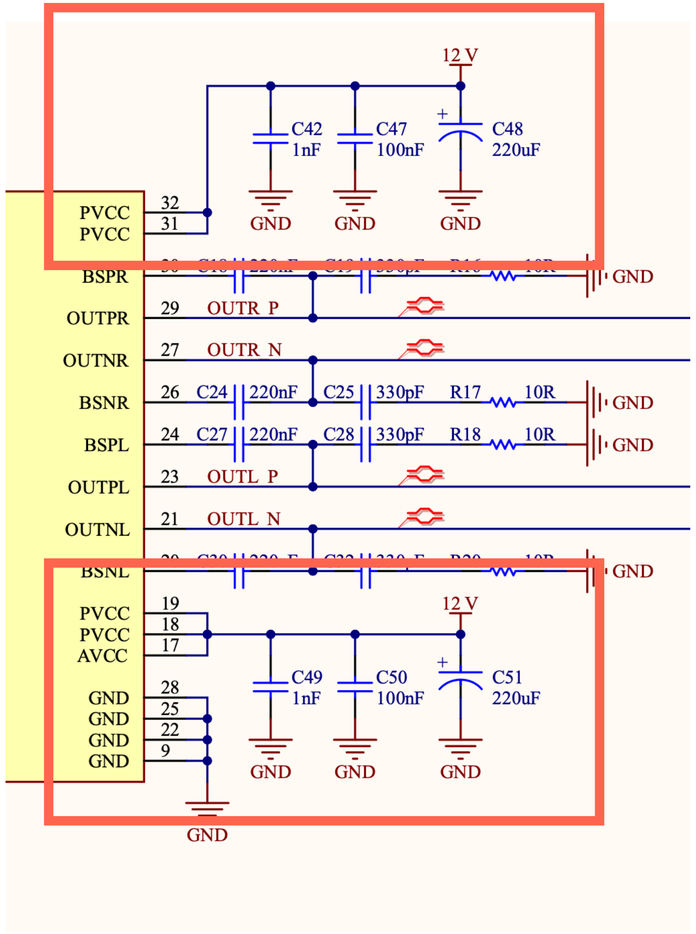
Tightly Packing Components (similar idea).



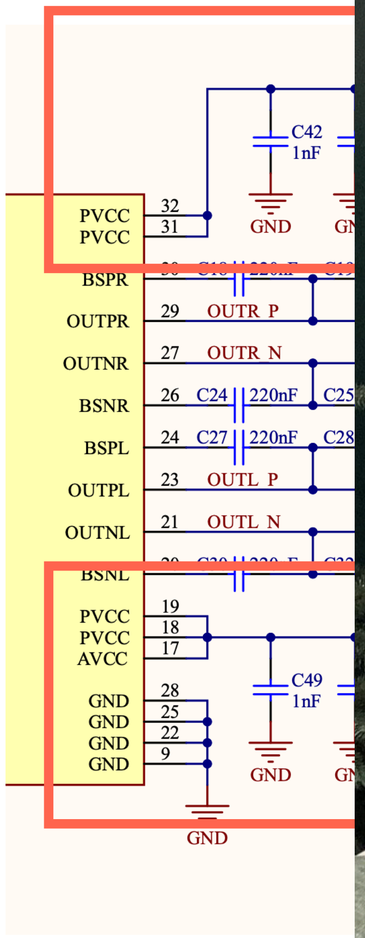
Let's use this circuit…

… and assume a footprint

@ MIT



What are these capacitors for? Why are they duplicates?



THE ART AND SCIENCE of PCB DESIGN

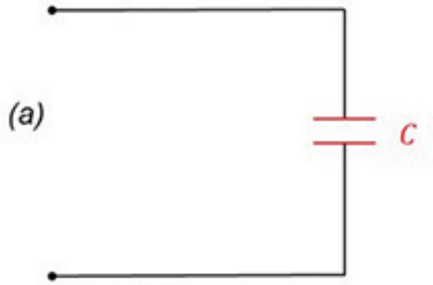
1/jw*C

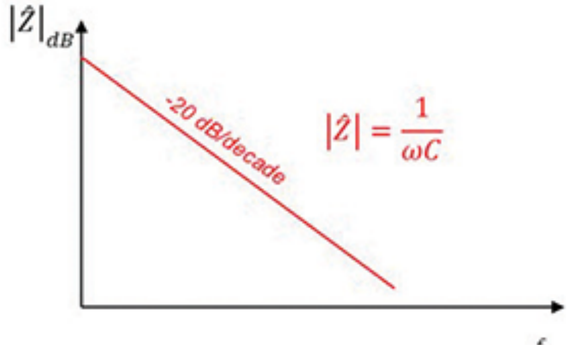
e
? Why
cates?

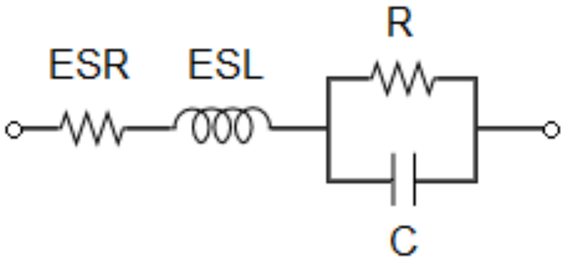
@ MIT

Bypass Capacitance!

https://incompliancemag.com/article/impact-of-a-trace-length-on-capacitor-frequency-response/

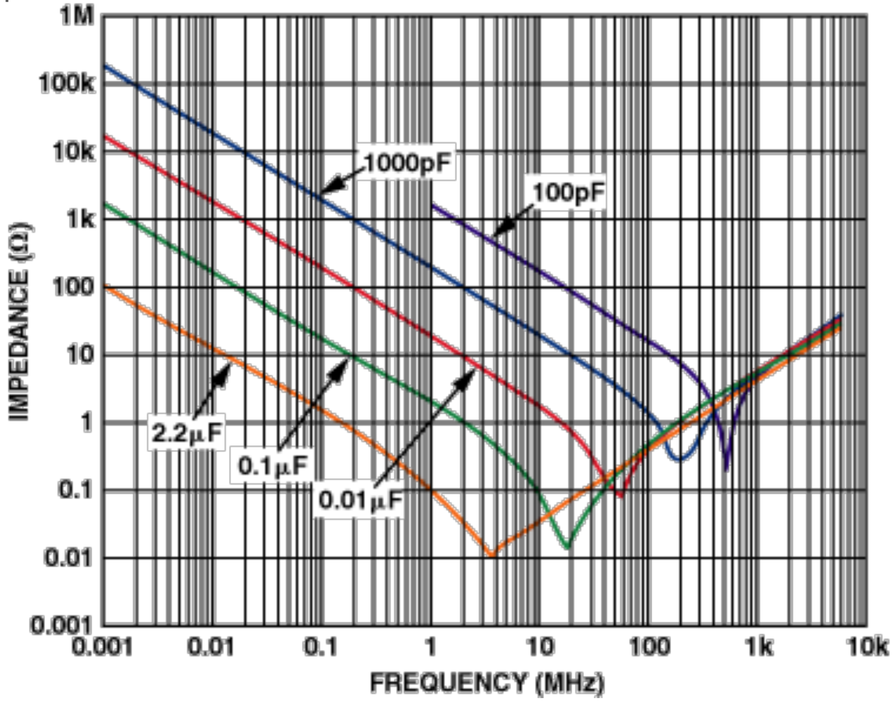






$$f = \frac{1}{2\pi\sqrt{C \cdot ESL}}$$

https://electronics.stackexchange.com/questions/3879/frequency-dependence-of-electrolytic-capacitors

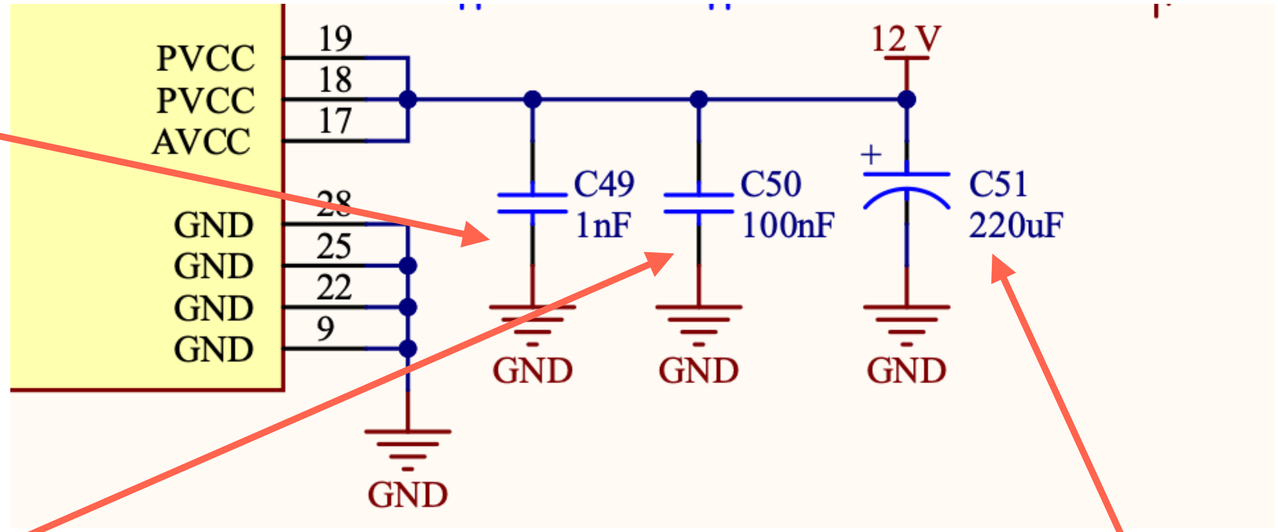


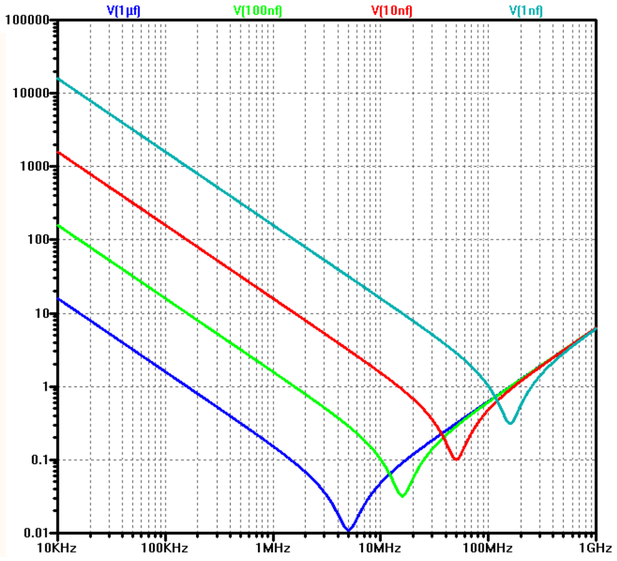
https://resources.altium.com/p/what-size-decoupling-capacitor-should-i-use-my-digital-ics

Bypass Capacitance!

https://electronics.stackexchange.com/questions/3879/frequency-dependence-of-electrolytic-capacitors

1nF capacitor for super high frequency noise





100nF capacitor for medium-high frequency noise

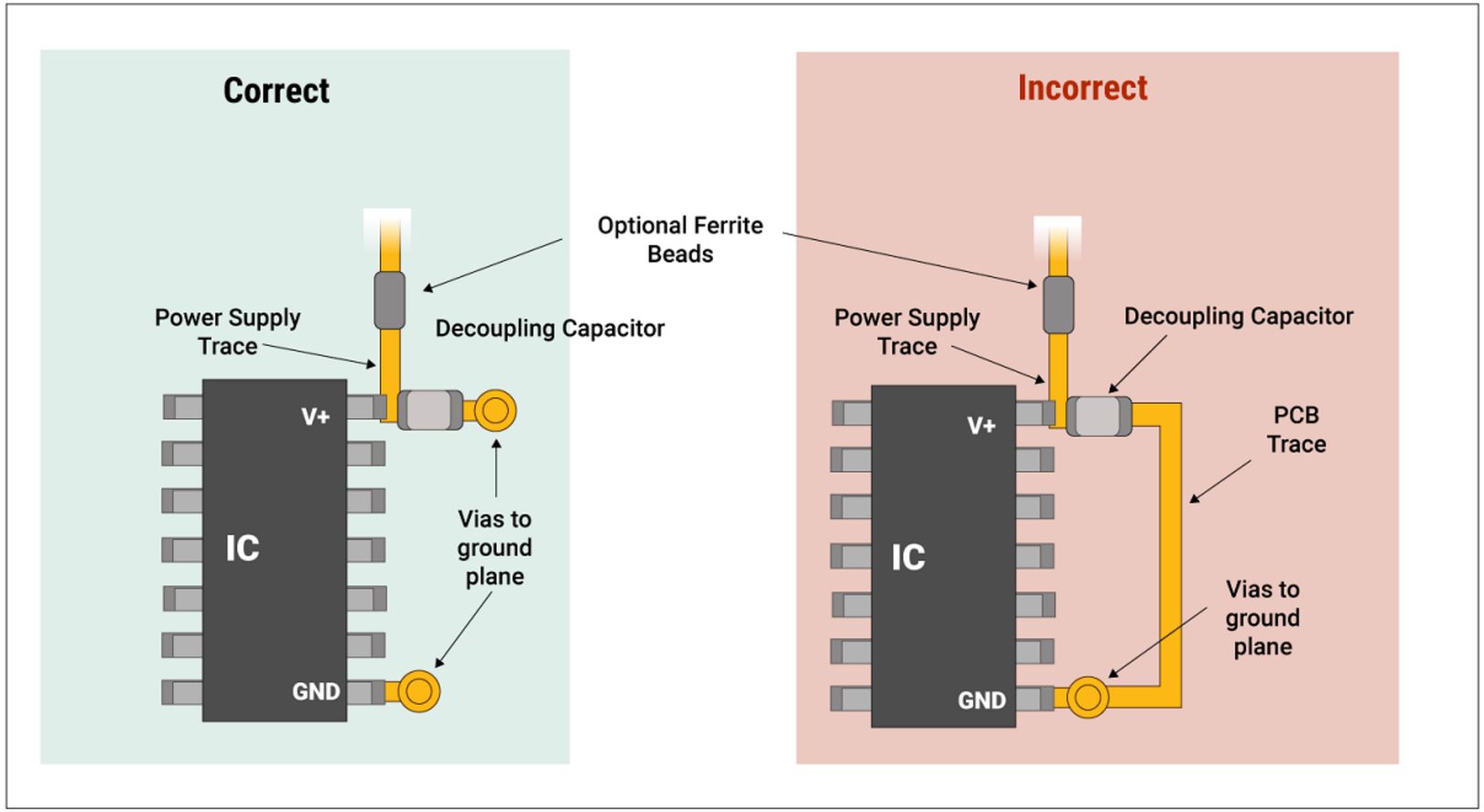
Large electrolytic capacitor with high ESR for low frequency noise

@ MIT

Location of Bypass.

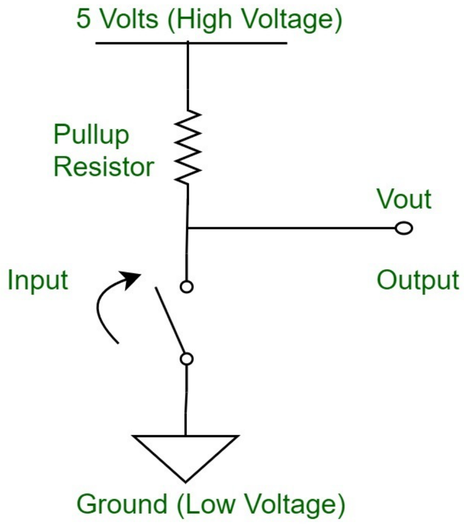
https://www.protoexpress.com/blog/decoupling-capacitor-use/

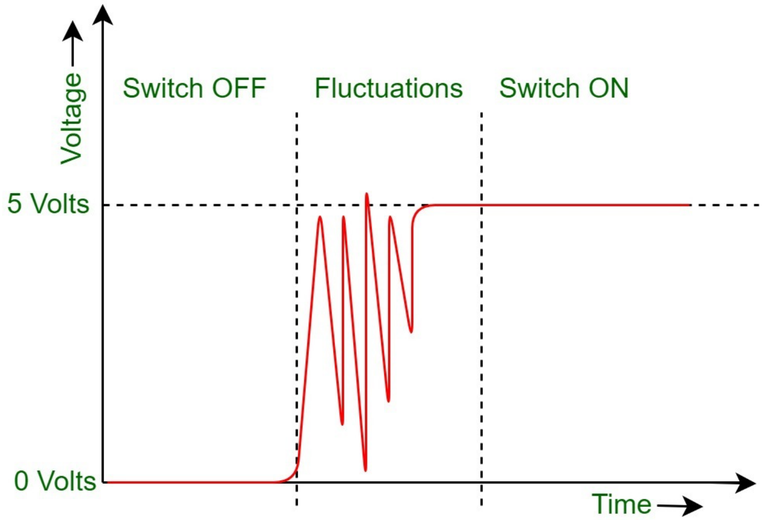
Both Links contain pretty good tutorials



https://www.protoexpress.com/blog/decoupling-capacitor-placement-guidelines-pcb-design/

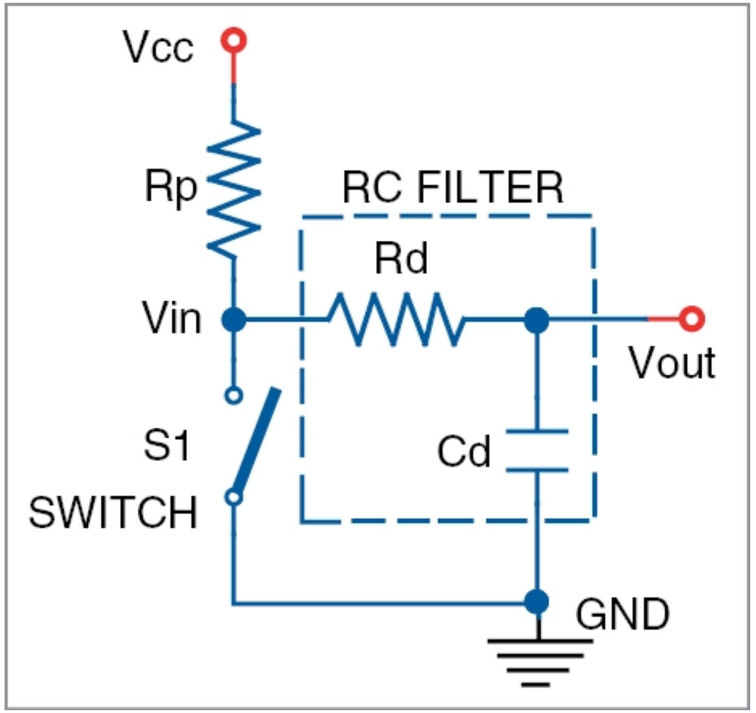
Location for Filtration / Debounce (and ESD).





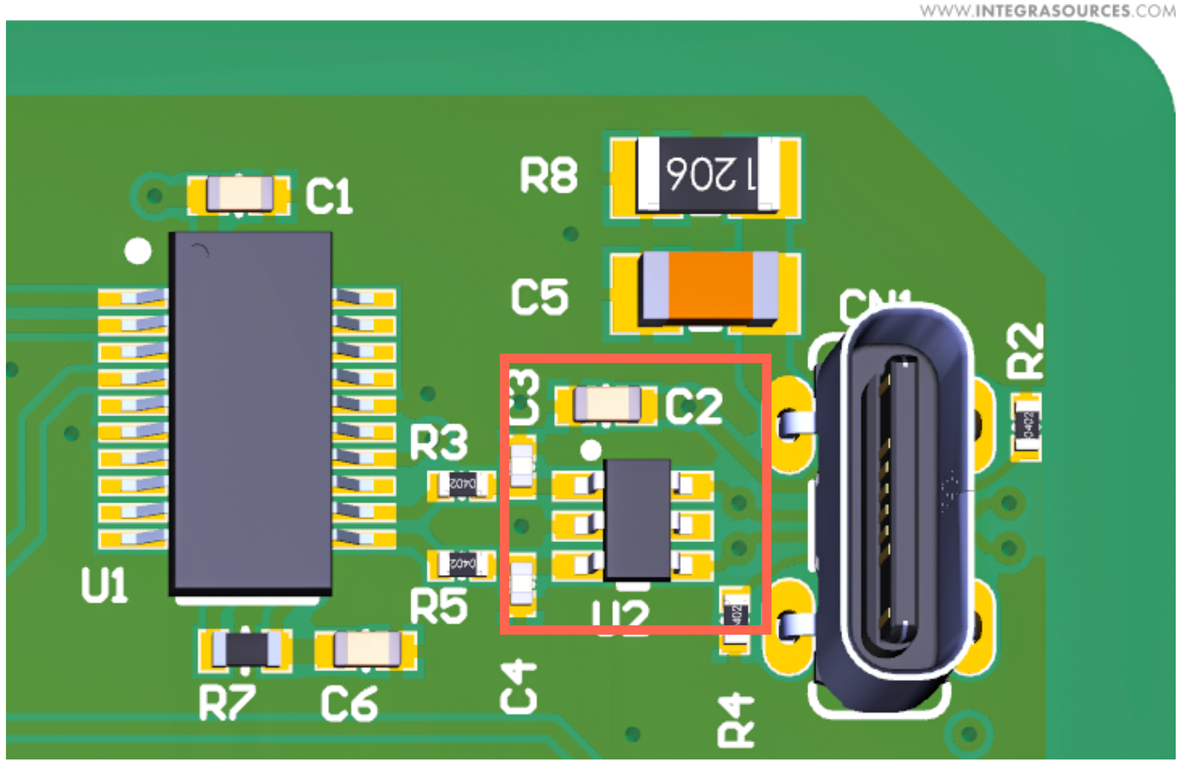
https://www.geeksforgeeks.org/switch-debounce-in-digital-circuits/

https://www.electronicsforu.com/electronics-projects/electronics-design-guides/switch-debouncer-working

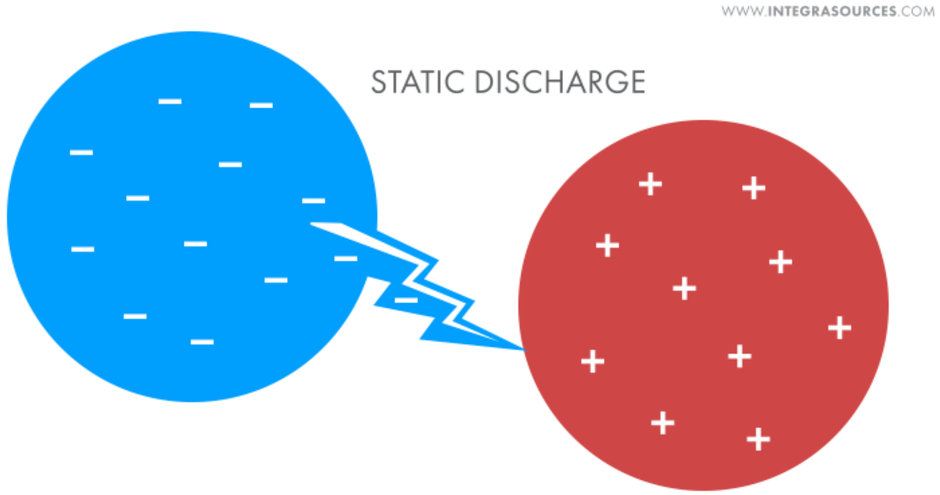


(Close to button)

ESD. (Close to USB / port / etc)



https://www.integrasources.com/blog/electronics-design-practices-prevent-eos-and-esd-damage/



What side of the board ‘mate?

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Most of the time, keep each sub-circuit on the same side of the board.

Manufacturing considerations as well.

For debugging or access or population you may only want components on one side of the board.

Still separate power and signal with X/Y distance, don’t put power on one side right on top of signal.

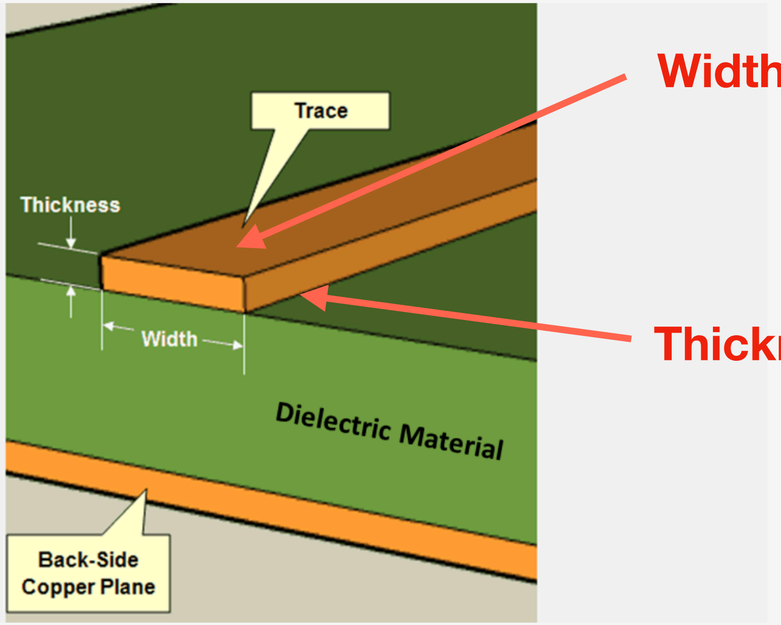
Routing the board, tools for connection!

THE ART AND SCIENCE OF PCB DESIGN

DO NOT USE AUTOROUTE. ITS BAD. ITS BAD. ITS BAD.

IF YOU DON’T KNOW WHAT AUTOROUTE IS. GOOD. STAY INNOCENT.

Calculating Trace Width + Spacing.



Width in (mil)

Thickness in (oz)

PCB trace structure

https://www.protoexpress.com/blog/trace-current-capacity-pcb-design/

1 oz Copper Thickness Conversion

1	oz	
1.37	mils (thousandths of an inch)	**To determine the thickness of 4 oz, simply multiply 1 oz thickness x 4.*
0.00137	inch	*1.37 mil x 4 = 5.48 mils = 4 oz*
0.0347	mm	
34.79	μm (micron/micro meter)	

https://www.pcbuniverse.com/pcbu-tech-tips.php?a=4

Calculating Trace Width + Spacing.

https://www.mclpcb.com/blog/pcb-trace-width-vs-current-table/

IPC Recommended Track Width For 1 oz cooper PCB and 10 °C Temperature Rise

Current/A	Track Width(mil)	Track Width(mm)
1	10	0.25
2	30	0.76
3	50	1.27
4	80	2.03
5	110	2.79
6	150	3.81
7	180	4.57
8	220	5.59
9	260	6.60
10	300	7.62

Max Current

You can calculate maximum current by using the formula $A = (T \times W \times 1.378\ [mils/oz/ft^2])$.

The values in this formula correspond with the following parameters:

- **A:** Cross-section area.
- **[mils2] T:** Trace thickness.
- **[oz/ft2] W:** Trace width.

Once you've worked through the previous equation, you'll determine the maximum current using $I_{MAX} = (k \times T_{RISE}^{b}) \times A^{c}$.

The fields for this formula are as follows:

- **[mils] I_{MAX}:** Maximum current.
- **[A] TRISE:** Maximum desired temperature rise.
- **[°C] k, b and c:** Constants.

Calculating Trace Width + Spacing.

https://www.mclpcb.com/blog/pcb-trace-width-vs-current-table/

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10	300	7.62

Resistance Calculation

When calculating trace resistance in your PCB, you'll begin by converting the cross-section area from [$mils^2$] to [cm^2] following the formula $A' = A * 2.54 * 2.54 * 10^{-6}$.

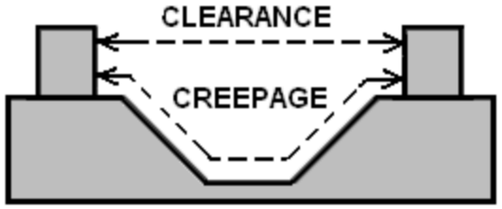
After working through the equation, you'll quantify the trace resistance using $R = (\rho * L / A') * (1 + \alpha * ({}^{T}_{TEMP} - 25\ °C))$.

The values in these formulas correspond with the following quantities:

- **T:** Trace thickness.
- **[oz/ft^2] W:** Trace width.
- **[mils] R:** Trace resistance.
- **[Ω] ρ:** Resistivity parameter.
- **[Ω · cm] L:** Trace length.
- **[cm] α:** Resistivity temperature coefficient.
- **[1/°C] $^{T}_{TEMP}$:** Trace temperature.

Calculating Trace Width + Spacing.

https://www.smps.us/pcbtracespacing.html



Electrical clearances and creepage for various types of insulation for mains up to 250VAC and working voltages up to 420V

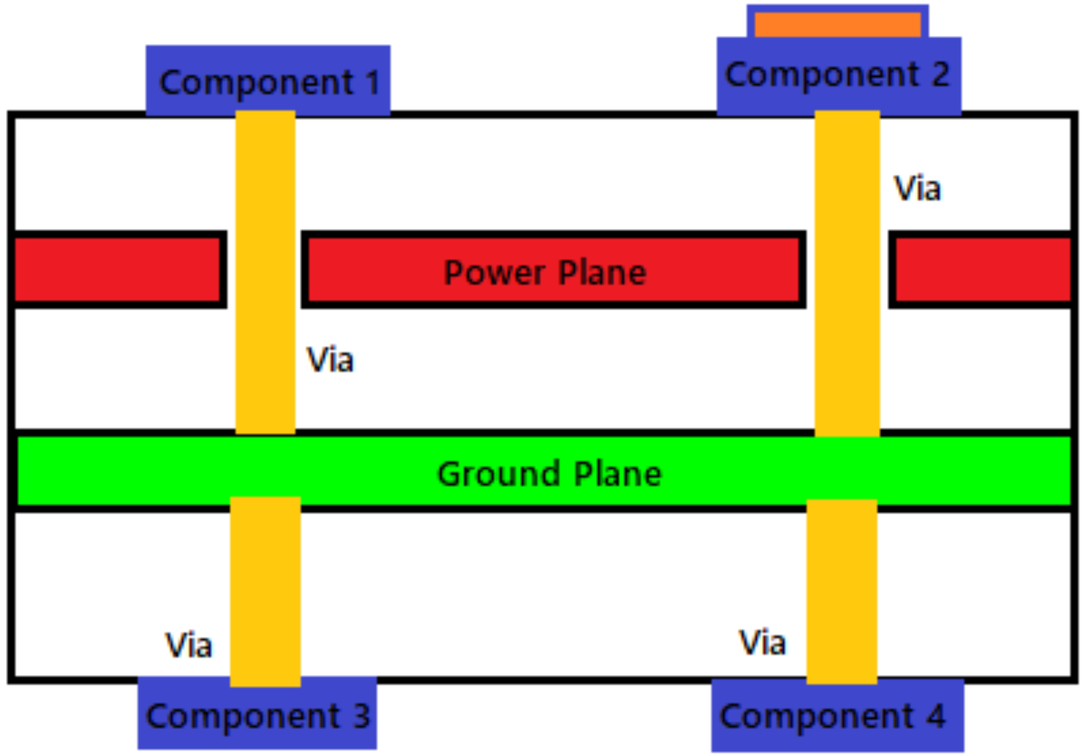
	Functional	Basic	Reinforced
Clearance	1.5	2	4
Creepage	3.2	3.2	6.4

Functional insulation- primary to primary and secondary to secondary;
Basic insulation- primary to chassis;
Reinforced insulation- primary to secondary.

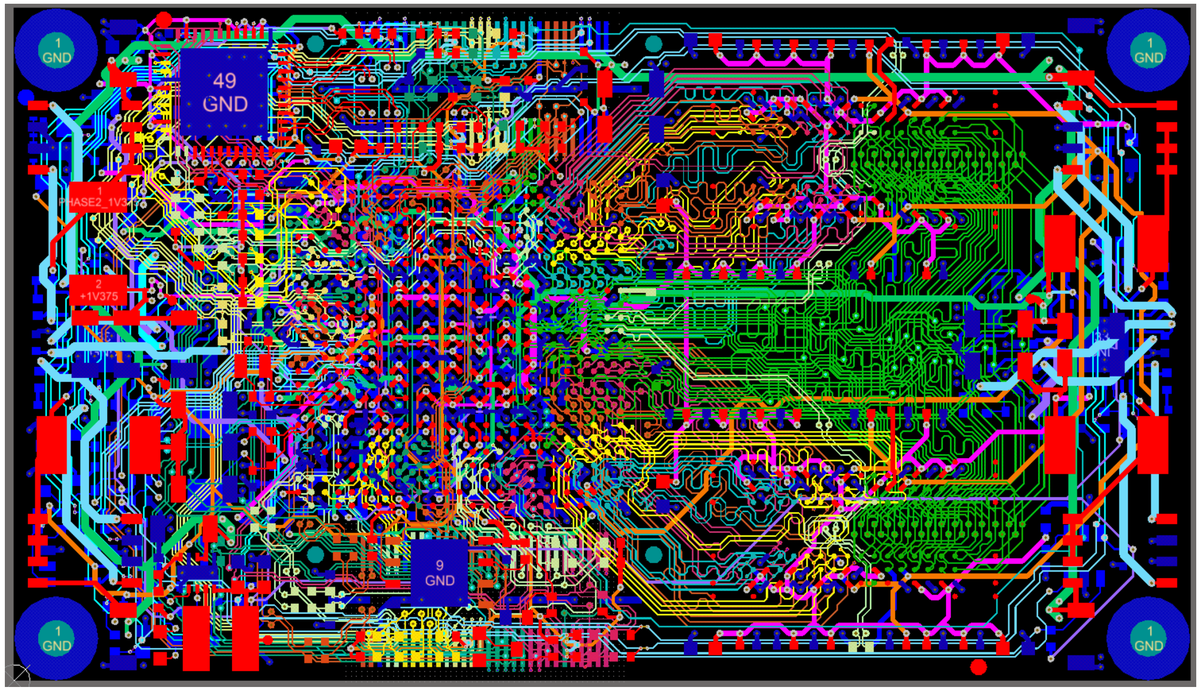
http://www.smps.us/

At atmospheric pressure, the breakdown strength of air is **~30 kV/cm**

Planes + the Layer-Stack-Manager.



https://welldoneblog.fedevel.com/2013/09/11/online-advanced-pcb-layout-course-by-motherboard-designer/



https://www.onelectrontech.com/pcb-layout-design-tips-grounding-considerations/

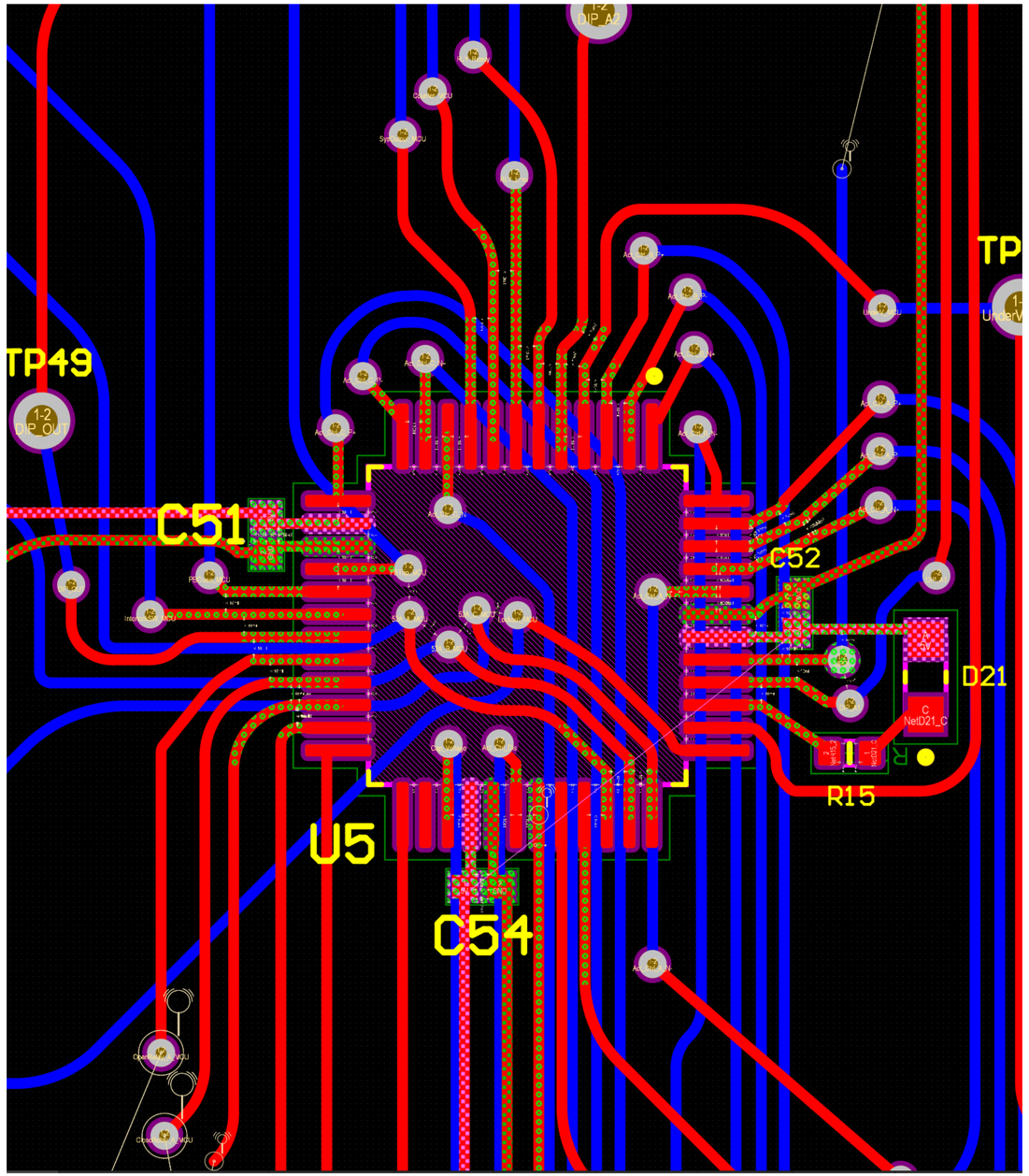
Planes + the Layer-Stack-Manager.

(Start w/ 2 layers and then increase as needed)

Vias.

Pretty common practice w/ signals going to a microcontroller.

Used to transition from layer to layer.

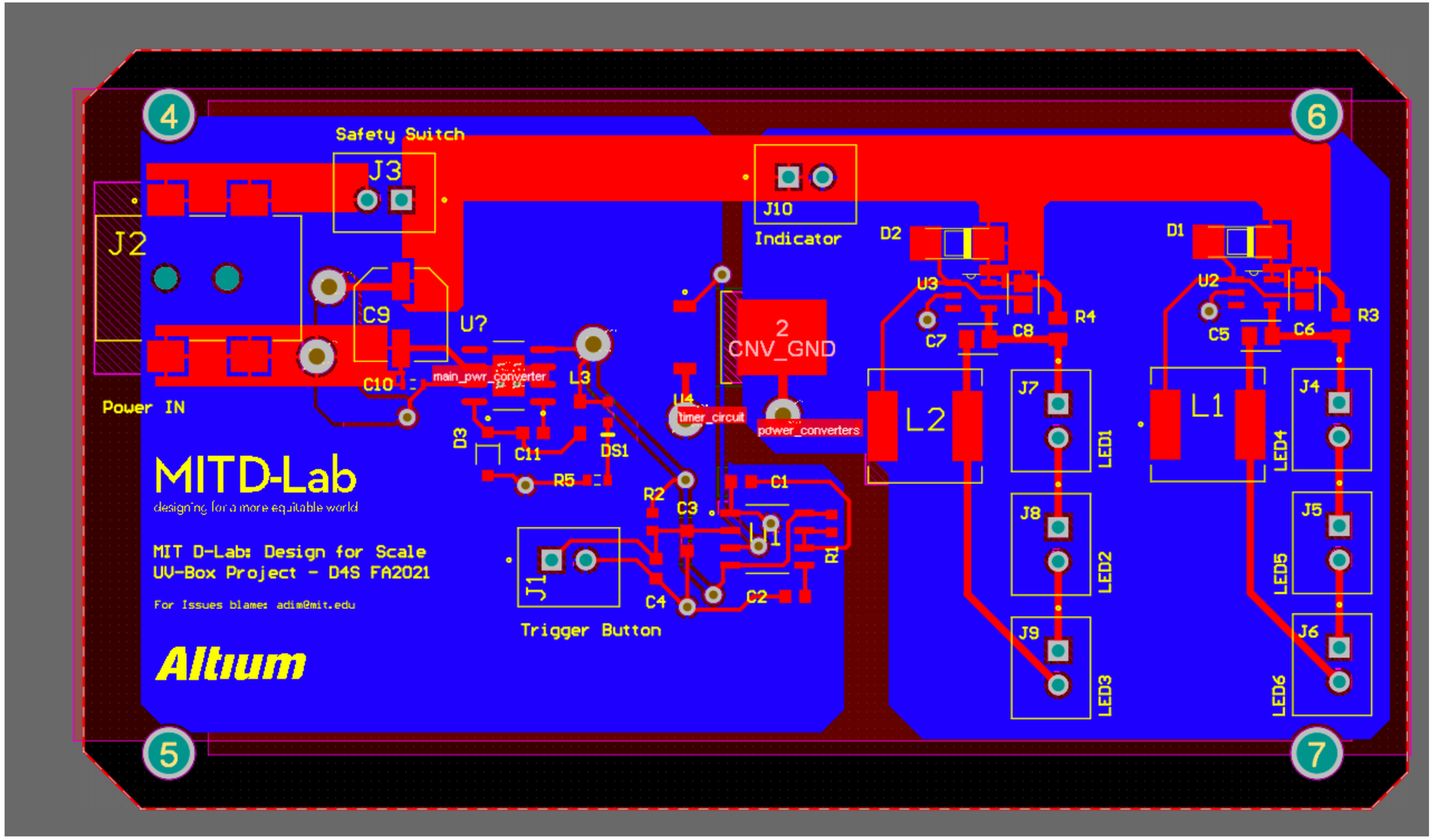


https://electronics.stackexchange.com/questions/604828/routing-traces-to-and-from-a-48-pin-microcontroller-becoming-a-mess

Pours, Pads, Polygons.

THE ART AND SCIENCE of PCB DESIGN

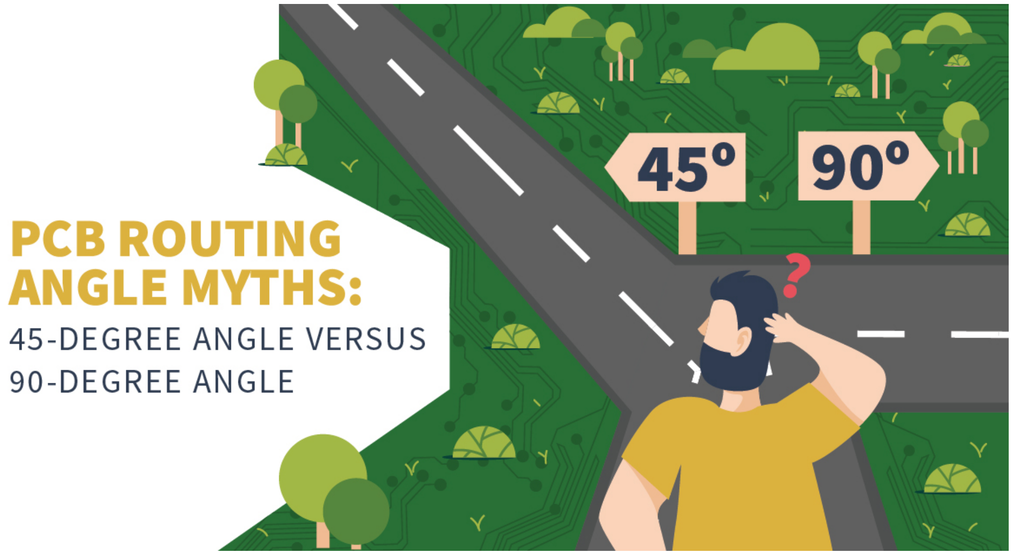
Better than running massive traces. Good way to get power around in a 2-layer board.



Layout considerations,

capacitors, debugging, parasitics.

Trace Shapes, Sharp Turns, EMI



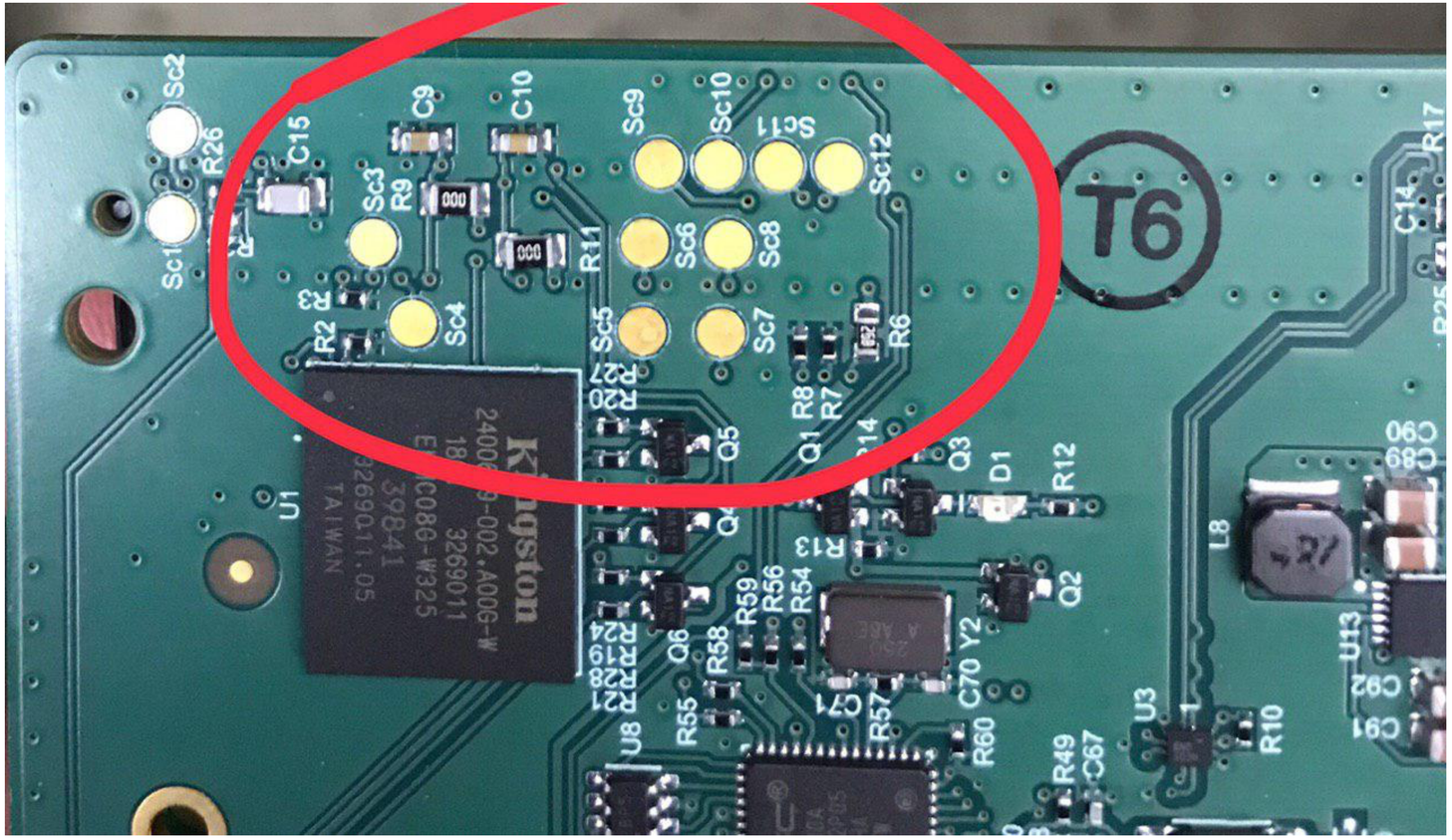
Engineers are often concerned about having right-angle PCB tracks on their circuit board shape due to the possibility of Electromagnetic Interference (EMI) radiated at sharp corners. The popular theory is that high-frequency signals emit Radio Frequency radiation at every 90° turn of the copper track. This mere assumption is enough for most hardware designers to eliminate any right-angle PCB routing from their track design or auto router software.

There is an exception--when you're designing ultra high-speed PCB ground plane in the range of 10 GHz or more, or you're involved in microwave designs that use traces with large widths of 100 mils. In such extreme applications, you actually need to worry about 90° corners. Otherwise, they should not present a major concern.

But the 45 deg corners do make a nicer looking board.

https://resources.altium.com/p/pcb-routing-angle-myths-45-degree-angle-versus-90-degree-angle

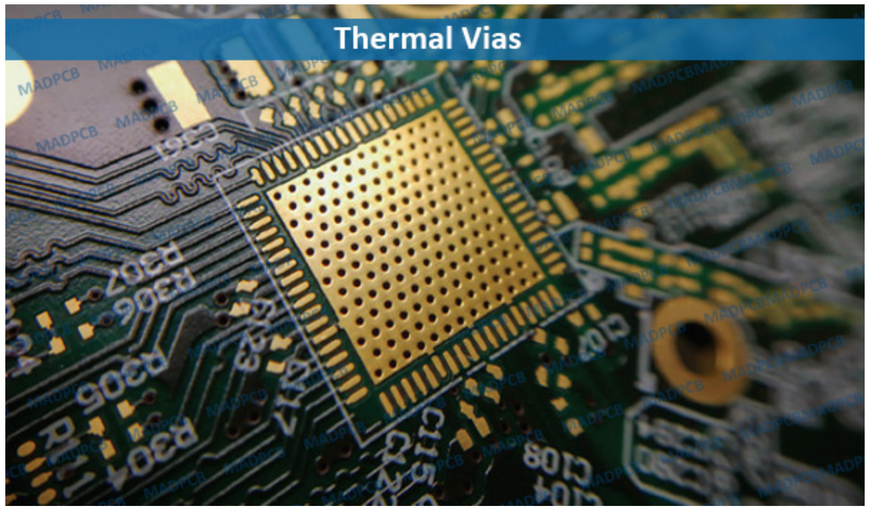
Debugging Considerations + Breakouts.



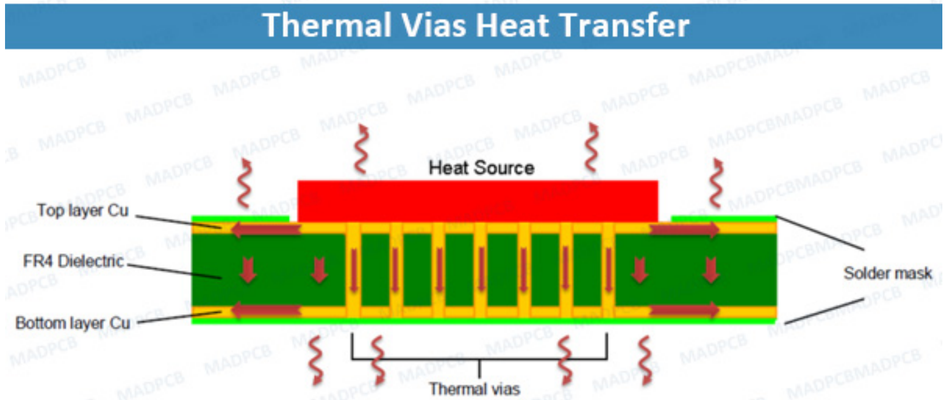
These are called TEST POINTS!

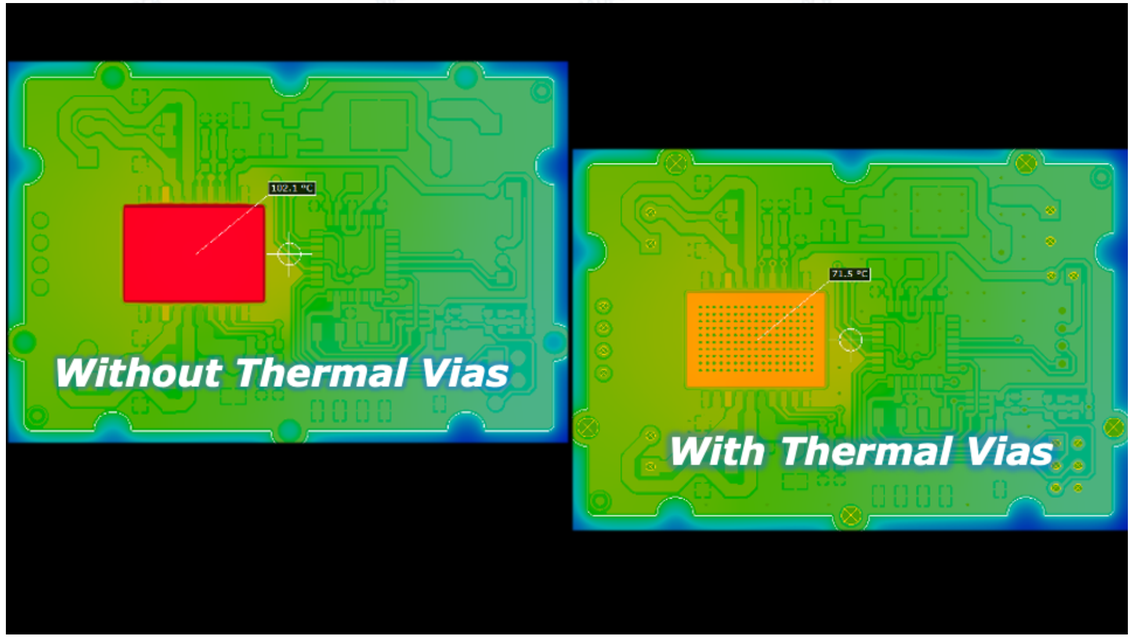
https://www.reddit.com/r/diyelectronics/comments/nynup4/any_way_to_permanently_connect_to_a_pcb_test_pad/

Thermals.



https://madpcb.com/glossary/thermal-vias/

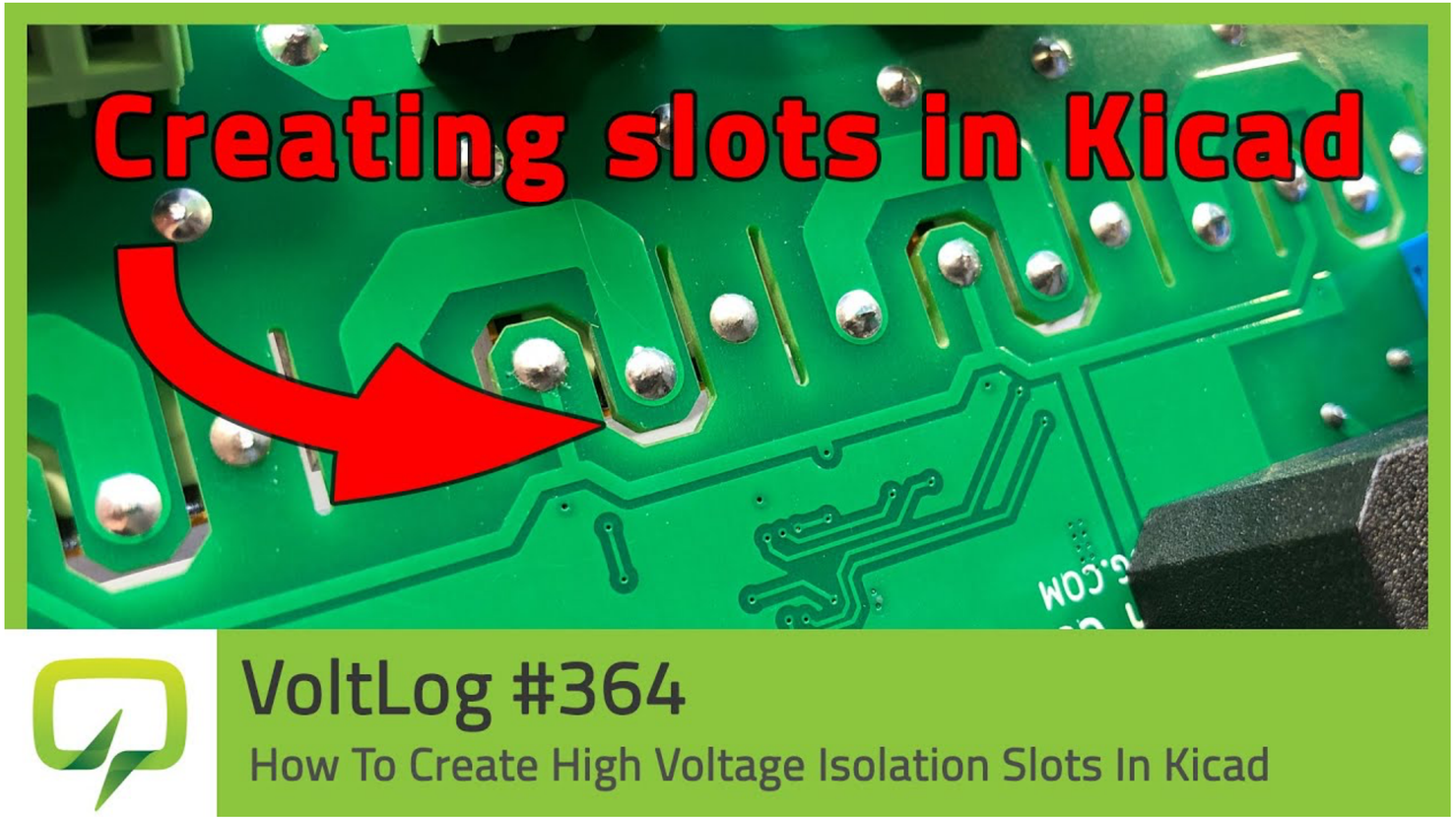




https://www.linkedin.com/pulse/thermal-vias-benefits-limitations-günther-schindler/

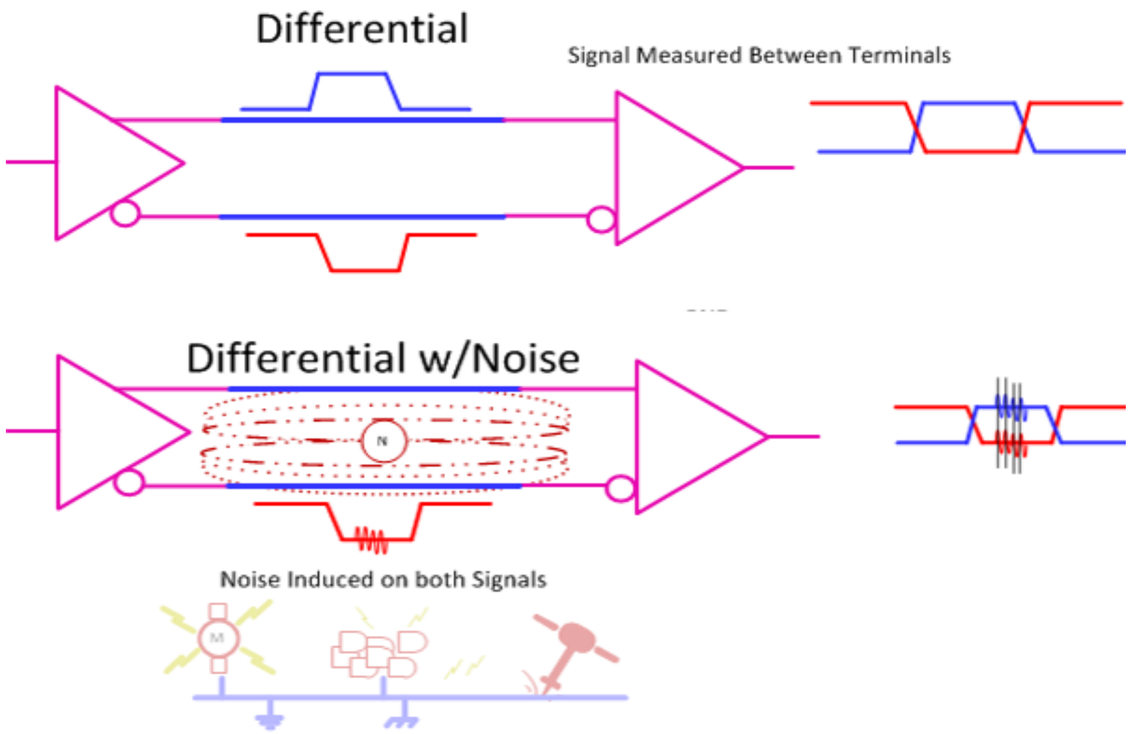
Isolation.

youtube.com/watch?v=BAJZpNDjiIA

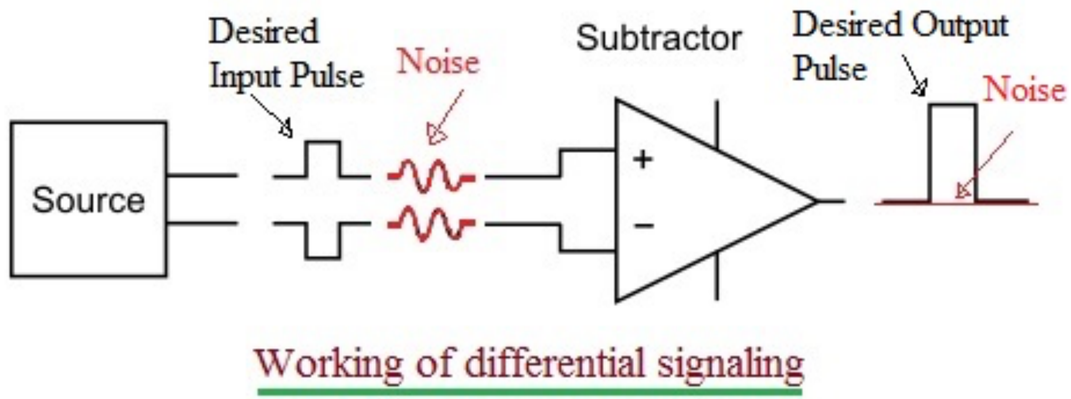


For separating large voltages over small distances we can use SLOTS in PCBs! This gives better isolation.

Differential Pairs + Signal Integrity.



https://hackaday.com/2016/03/29/when-difference-matters/



https://www.rfwireless-world.com/Terminology/Advantages-and-Disadvantages-of-differential-signaling.html

Connectors.

(Race-spec series)

Connectors should lie at the edge of the board

Mechanical Interlocking Connectors - connector takes forces, pins transmit signal

NO WIRES OVER THE BOARD!!!

Connectors is a whole science —> https://www.rbracing-rsr.com/wiring_ecu.html

Manufacturing Considerations + Board Shape.

THE ART AND SCIENCE of PCB DESIGN

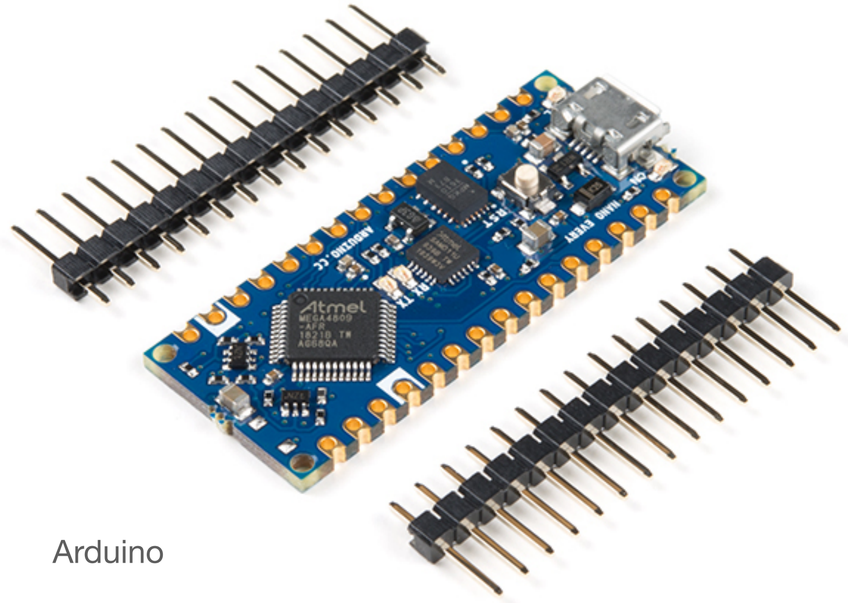
Cost —> layers add cost

Size —> size adds cost

Automated population —> two sided is more expensive than one sided

Trace spacing and width —> also factors

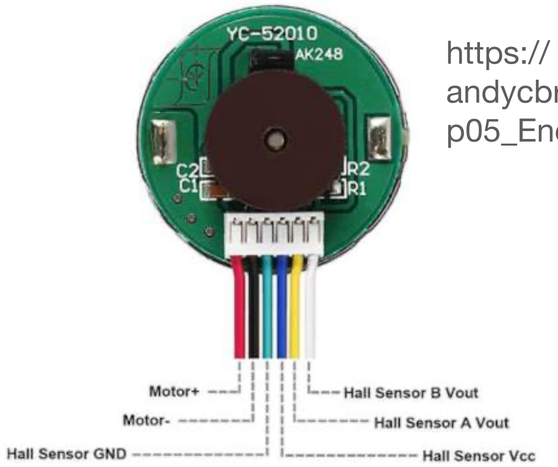
Manufacturing Considerations + Board Shape.



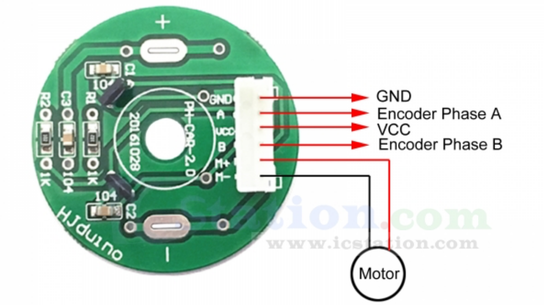
Arduino

https://www.eurocircuits.com/pcb-design-guidelines/edge-connectors/

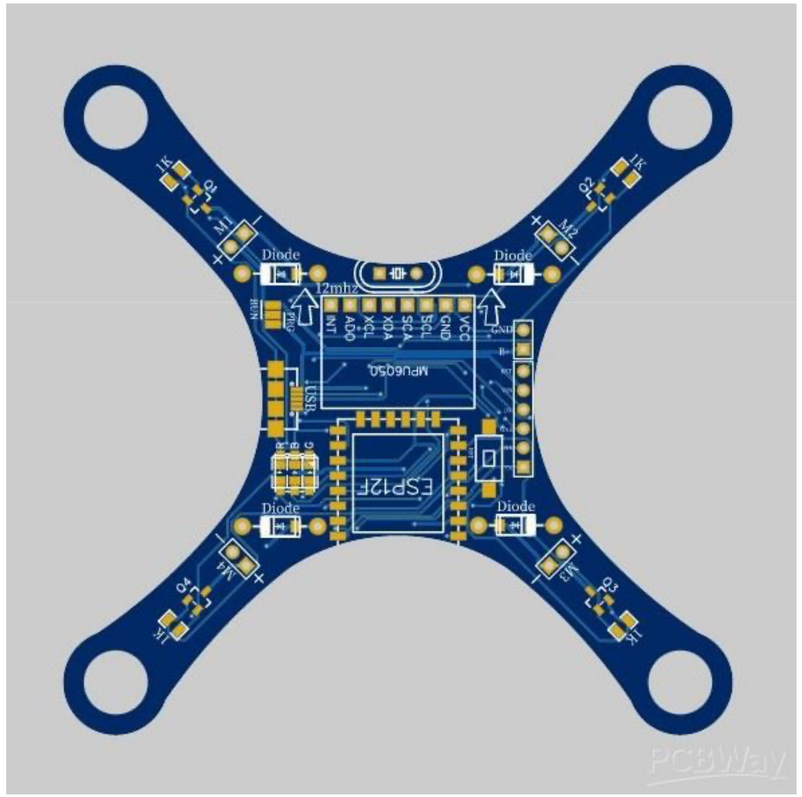
Mechanical Layers, Labeling, Naming, Blaming.



https://
andycbruce.com/
p05_EncoderDrvr.html



https://www.icstation.com/motor-phase-incremental-hall-sensor-encoder-magnetic-coding-speed-module-control-p-16006.html



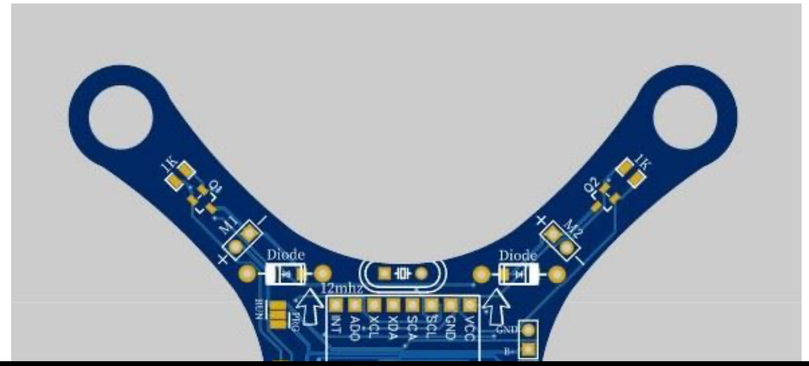
https://www.pcbway.com/blog/PCB_Design_Tutorial/How_To_Create_PCB_For_Drone.html

youtube.com/watch?v=-BDCmwNssiw

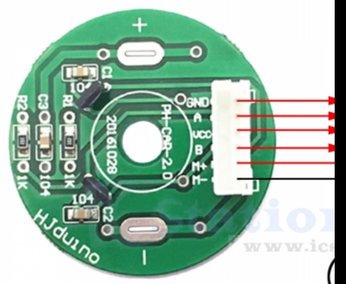
THE ART AND SCIENCE of PCB DESIGN

@ MIT

Mechanical Layers, Labeling, Naming, Blaming.

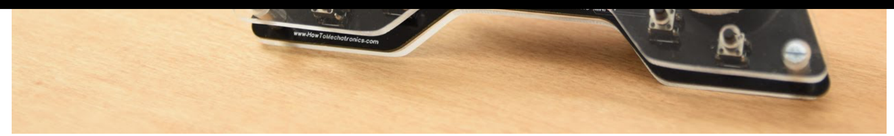


https://www.pcbway.com/
Tutorial/
CB_For_



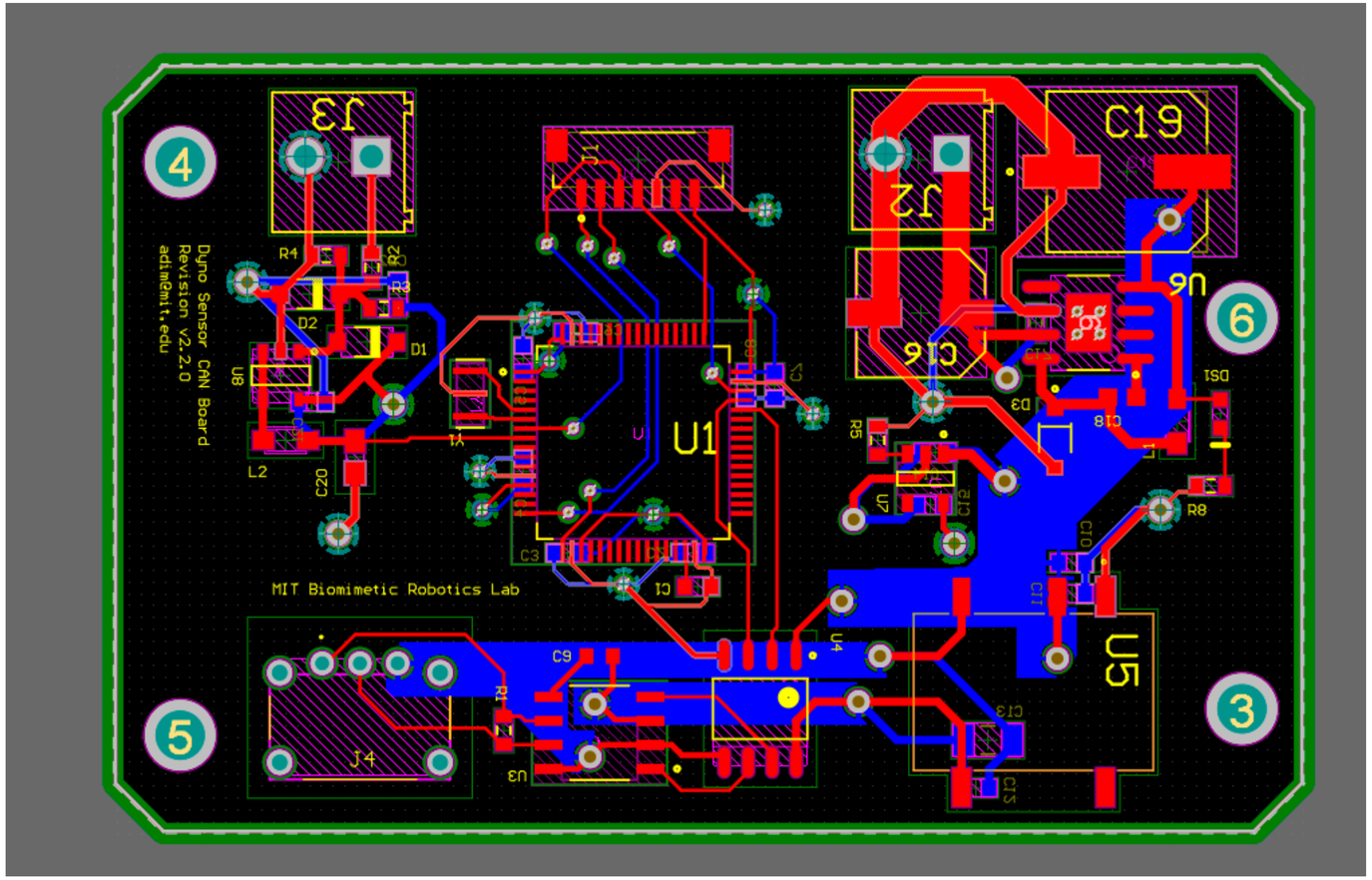
watch?v=-

Tradition is to put your name and email on a PCB if you've made it so the person debugging it knows who to blame when it goes wrong ;D

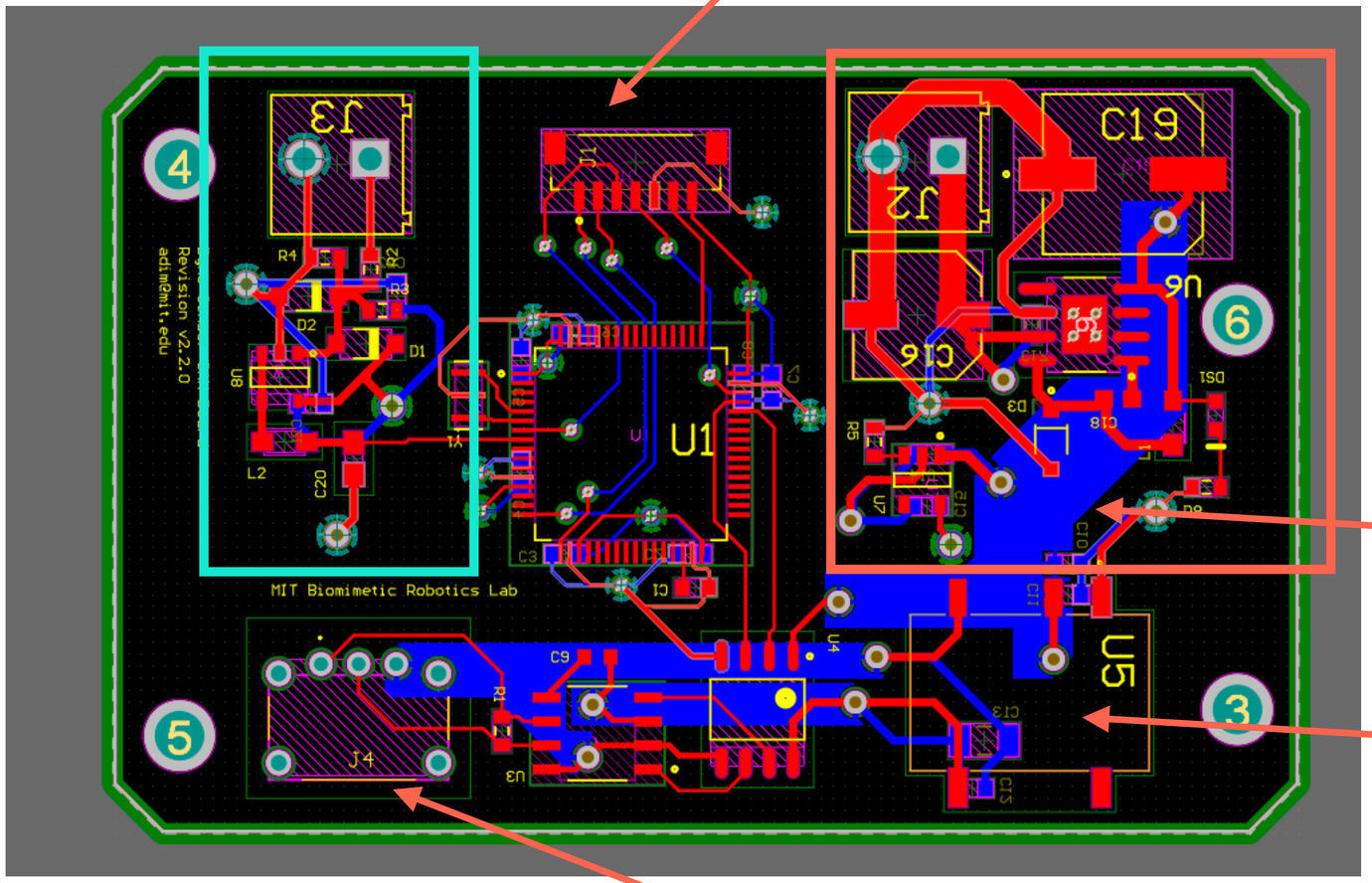


Layout case studies, a few boards (simple to complex).

Torque-Sense CAN Board.



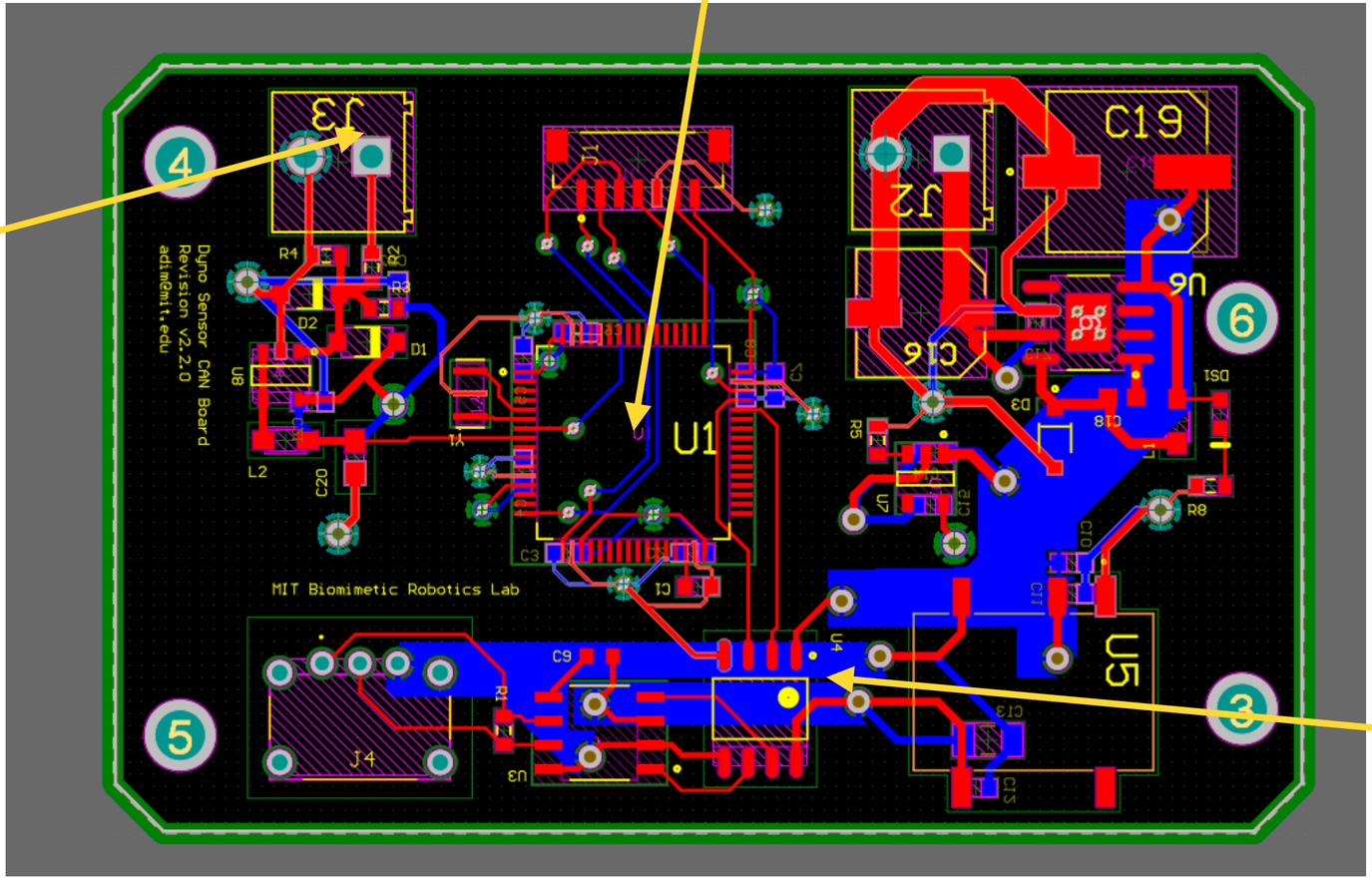
Torque-Sense CAN Board.



Torque-Sense CAN Board.

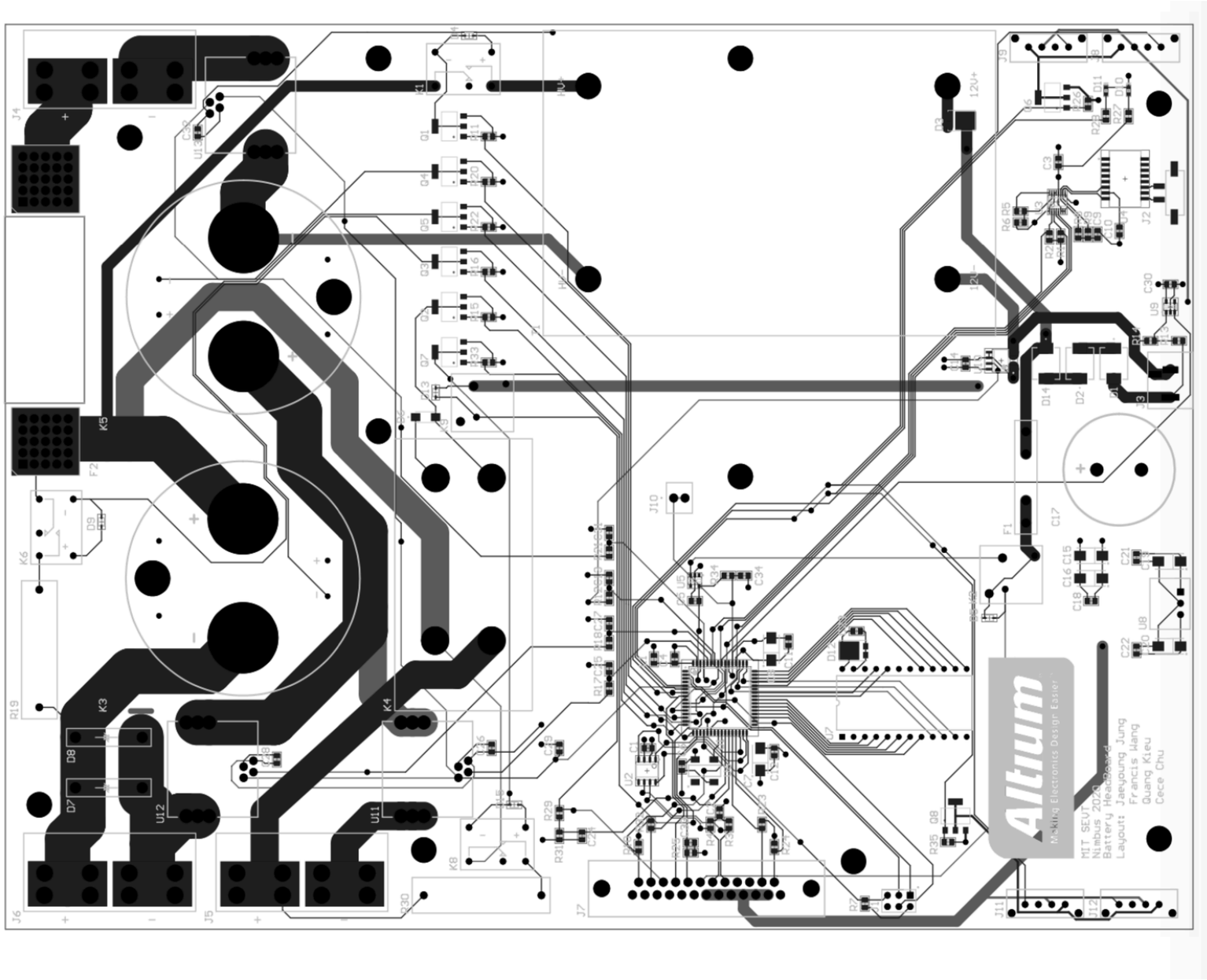
BAD —> BYPASS UNDER THE BOARD, SHOULD BE ON TOP

SCREW TERMINAL FOR SENSOR, COULD BE BETTER, SCREW TERMINALS HAVE A RESISTANCE



BAD —> CAN NOT ROUTED AS A DIFF PAIR

Solar Car BMS.



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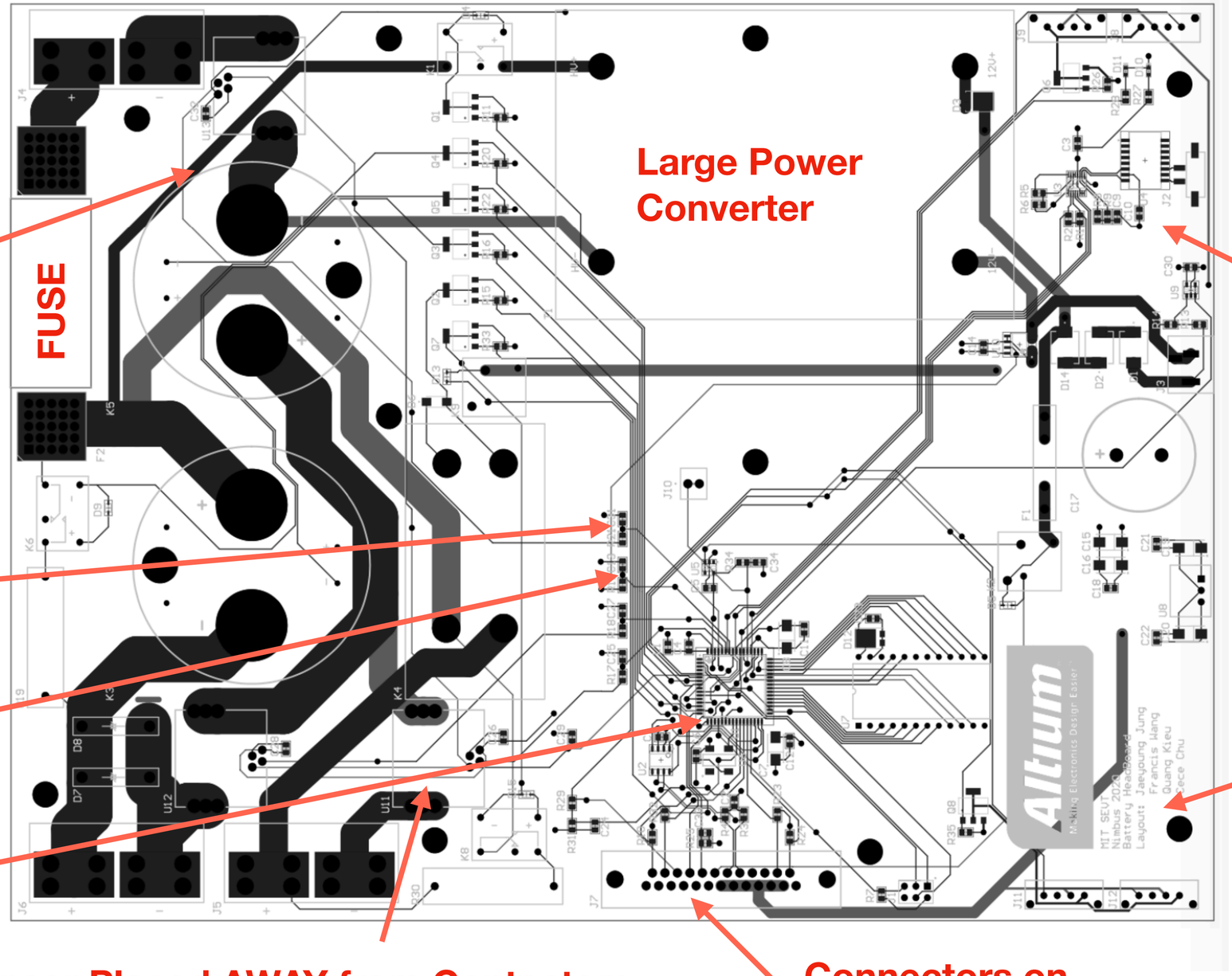
Solar Car BMS.



Power

Large Power Converter

Differential Communica-tions

Filtering for Current Sensors

Test Point for Current Sensor

Microcontroller w/ Bypass

Blame Names

Current Sensor Placed AWAY from Contactors

Connectors on Edges

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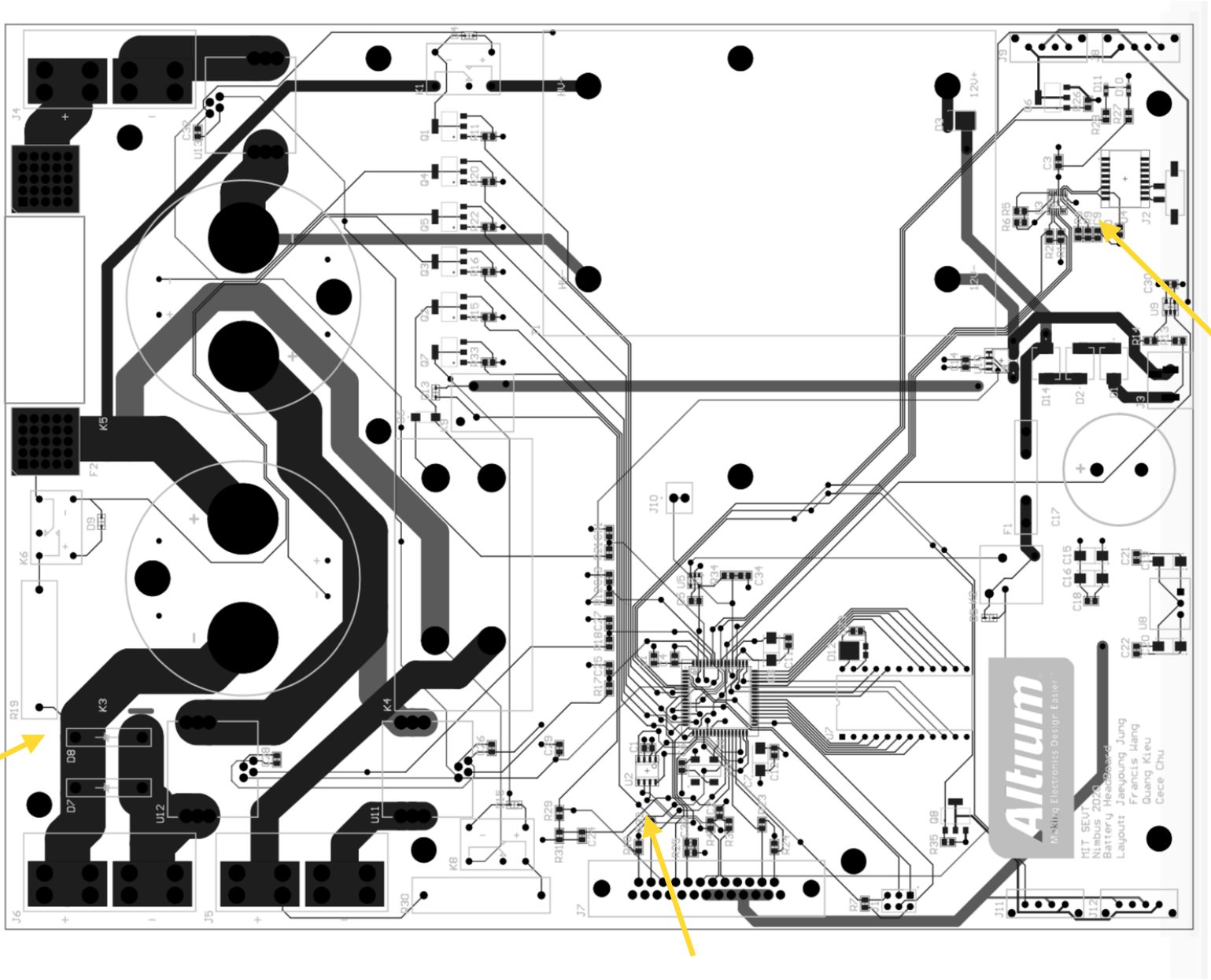
Solar Car BMS.

(Probably OK because of transmission speeds but diff pair is always better)



ISO-SPI NOT ROUTED AS A DIFF PAIR

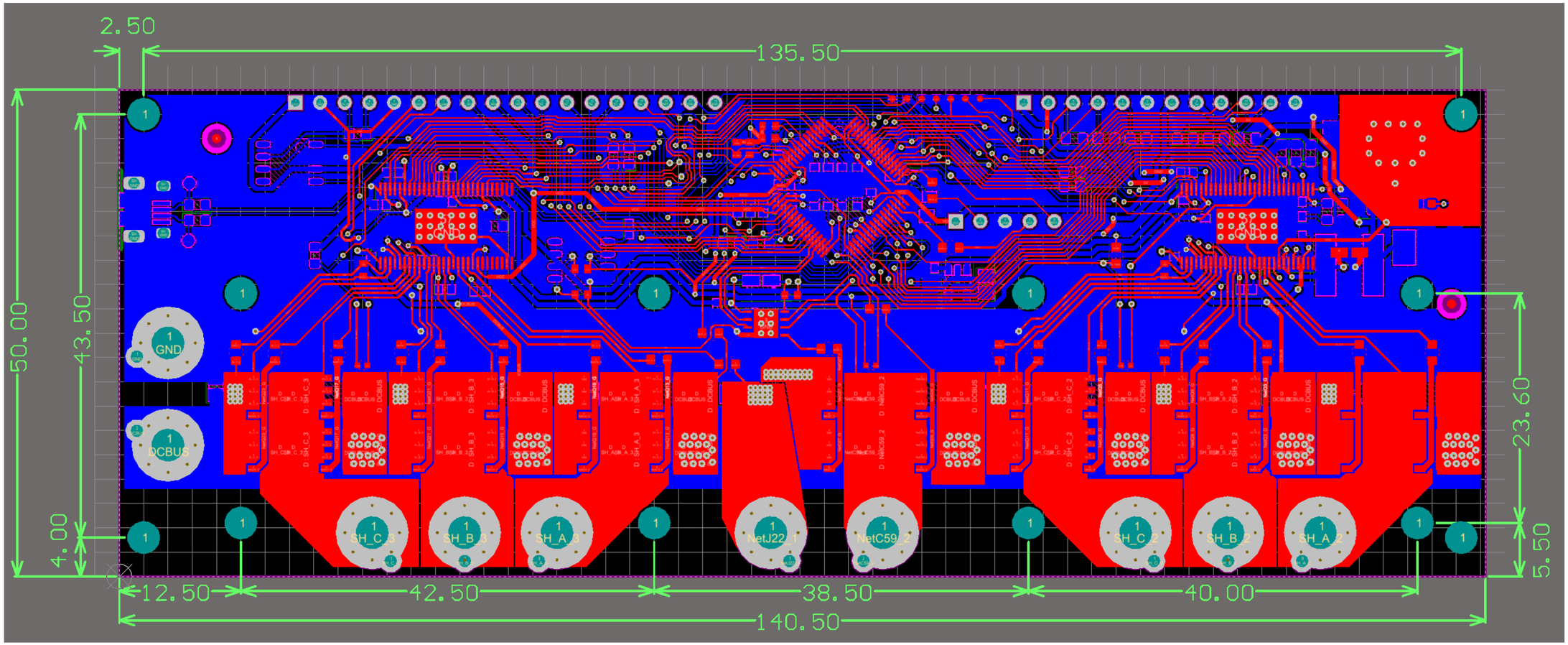
Could probably have used copper pours instead of large traces

CAN BUS NOT ROUTED AS A DIFF PAIR

THE ART AND SCIENCE of PCB DESIGN

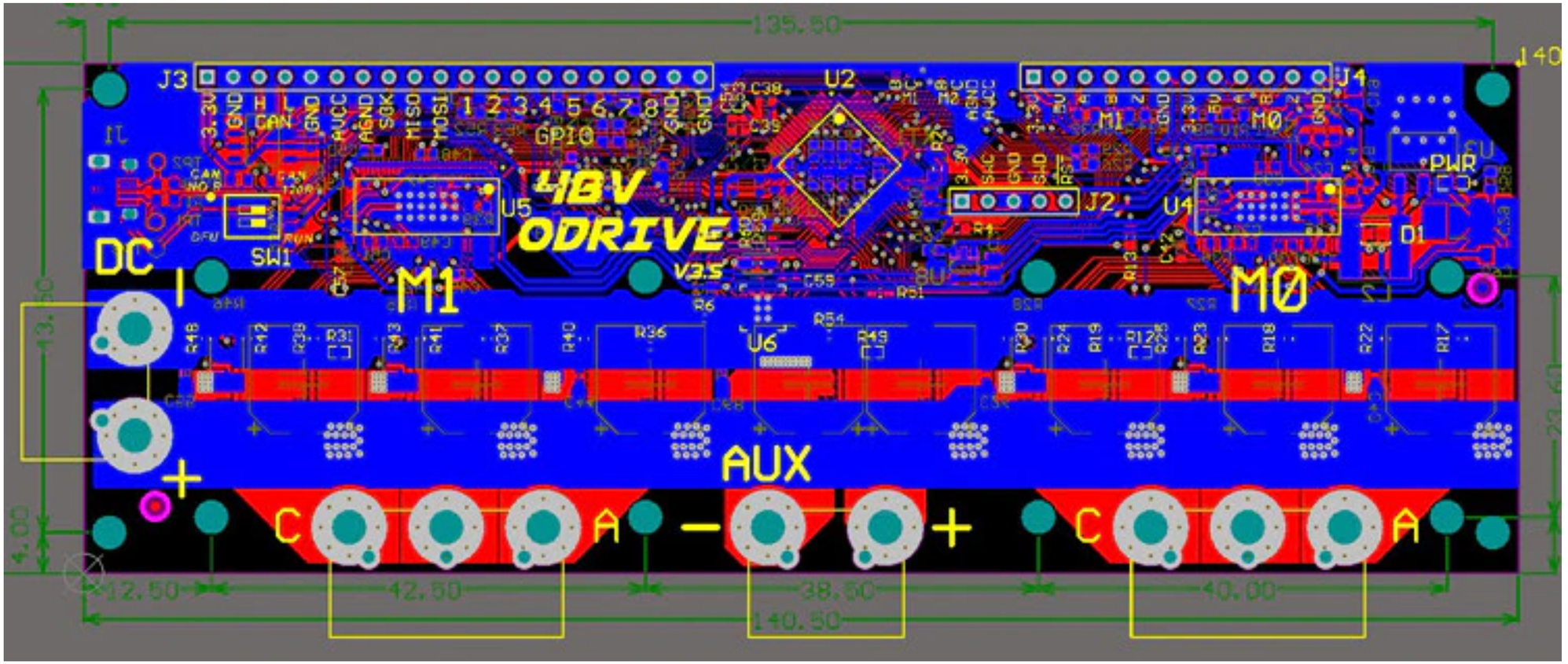
Detailed case study, Ben Katz motor controller in Eagle.

O-Drive MC V3.1 Layout!



@ MIT

O-Drive MC V3.1 Layout!



@ MIT

O-Drive MC V3.1 Layout!