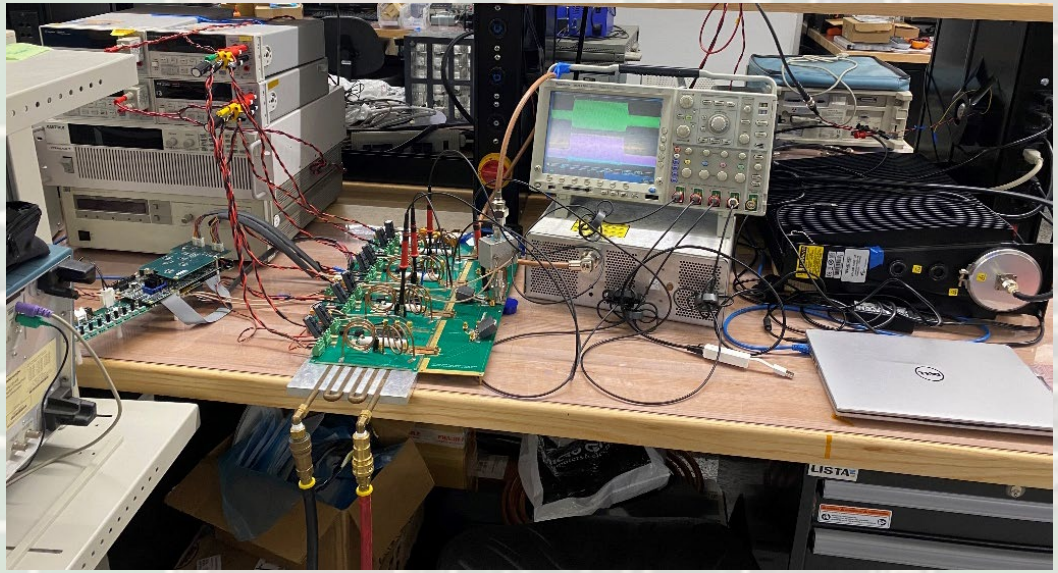
Massachusetts Institute of Technology
Power Electronics Research Group

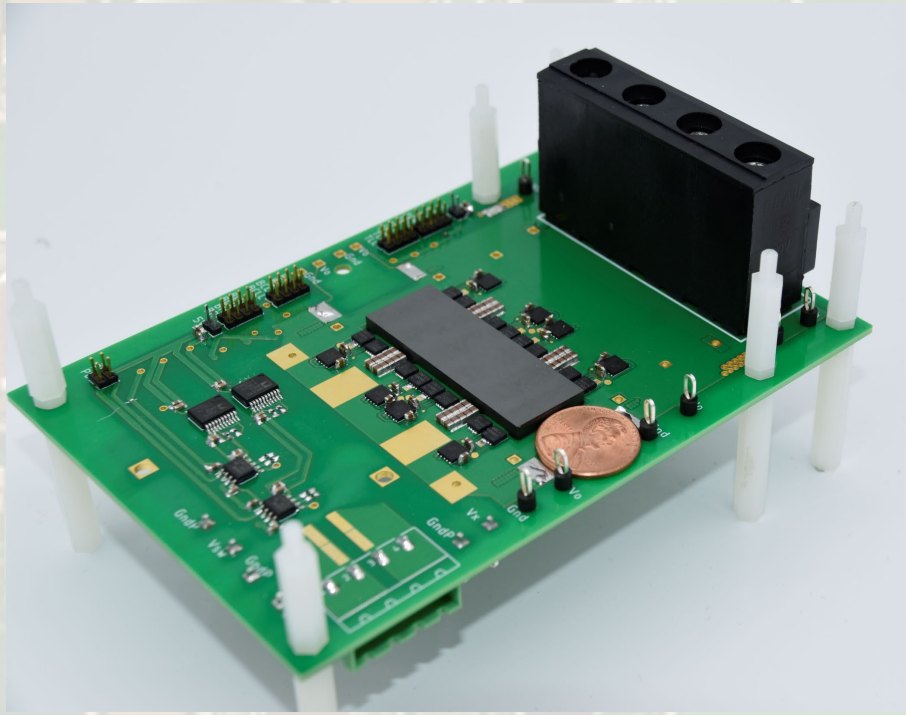
Some Notes on Printed Circuit Board Design for Power Circuits

MIT IAP Class

24 January 2025

David Perreault





Some Relevant Standards and Guidelines

- IPC-2221A Generic Standard on Printed Board Design
  - (2020 version) - Lots of useful information
  - Widely applied, but many companies also have their own internal standards
- MIL-STD-275E Printed Wiring for Electronic Equipment
  - Military standard from 1984 – dated but still has useful information
- UL 60950-1 Information Technology Equipment Safety
- R. Tarzwell & K. Bahl, "High Voltage Printed Circuit Design & Manufacturing Notebook," Sierra Proto Express, Nov. 4, 2004
- G.J. Wheeler, "The Design of Electronic Equipment," Prentice-Hall, 1972
  - An oldie but a goodie. Lots of useful information on pcb design
- Texas Instruments AN-2020 "Thermal Design By Insight, Not Hindsight"
  - Useful information on PCB heat transfer/heatsinking
- E. Persson, "Optimizing PCB Layout for HV GaN Power Transistors," IEEE Power Electronics Magazine, June 2023.

Current Carrying in PCB traces

- In designing power circuits, we often need to carry high currents. A key limitation is heating
- Conductor thickness selected as part of pcb design; conductor width selected to help with high current traces
  - Copper weights of 0.5 oz/ft^2 (17 µm thick) or 1 oz/ft^2 (34 µm thick) are typical
  - 2-4 oz/ft^2 copper weights are very widely available for power traces, and some manufacturers can provide VERY heavy copper, to > 15 oz/ft^2.
  - High-weight (etched) copper does provide limitations in trace aspect ratios, affecting achievable trace widths, spacing, etc.
  - Combinations of plating and etching can be used to provide extreme copper weights by some manufacturers (>> 20 oz/ft^2.)

Trace width selection

- **Various guidelines have been generated for how to size (e.g., width) of conductors for current carrying based on allowed temperature rise**
  - **e.g., IPC2221A Section 6.2**
- **Typical FR4 circuit board material limited to 130° C**

6.2 Conductive Material Requirements The minimum width and thickness of conductors on the finished board **shall** be determined primarily on the basis of the current-carrying capacity required, and the maximum permissible conductor temperature rise. The minimum conductor width and thickness **shall** be in accordance with Figure 6-4 for conductors on external and internal layers of the printed board.

$$I = k\Delta T^{0.44} A^{0.725}$$

Where I = current in amperes, A = cross section in sq. mils, and ΔT = temperature rise in °C and k is a constant such that:

k = 0.048 for outer layers
k = 0.024 for inner layers

The conductor's permissible temperature rise is defined as the difference between the maximum safe operating temperature of the printed board laminate material and maximum temperature of the thermal environment to which the printed board will be subjected. For convection-cooled

Trace width selection

- Various guidelines have been generated for how to size (e.g., width) of conductors for current carrying based on allowed temperature rise
  - e.g., IPC2221A Section 6.2
- External layer example:
  - Chart from IPC2221A Section 6.2 Fig. 6-4 “Conductor Thickness and Width for Internal and External Layers”

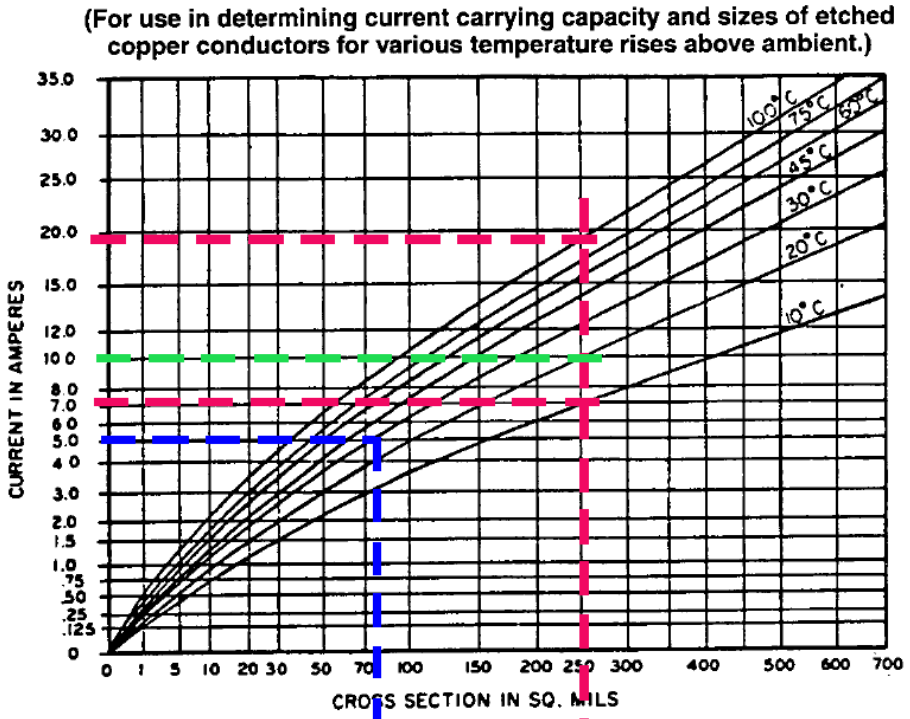


Figure A External Conductors

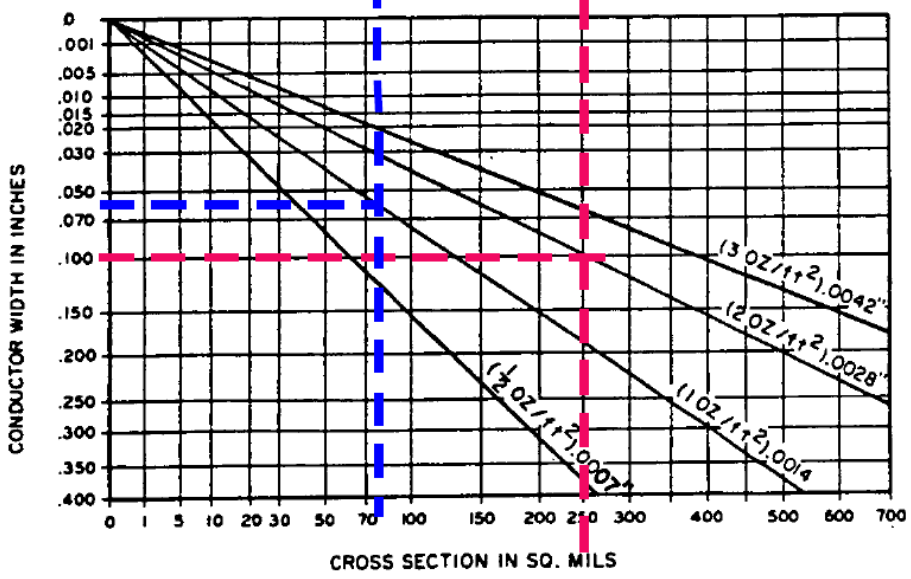


Figure B Conductor width to cross-section relationship

(For use in determining current carrying capacity and sizes of etched copper conductors for various temperature rises above ambient.)

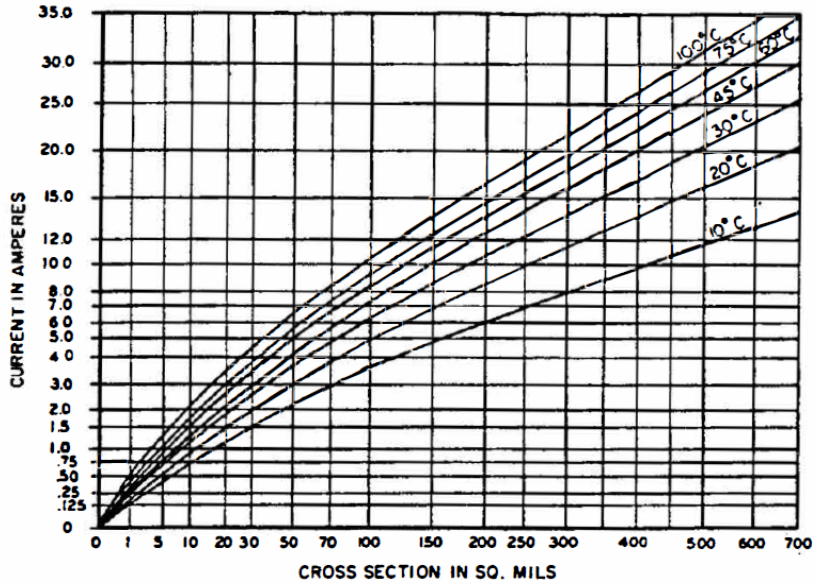


Figure A External Conductors

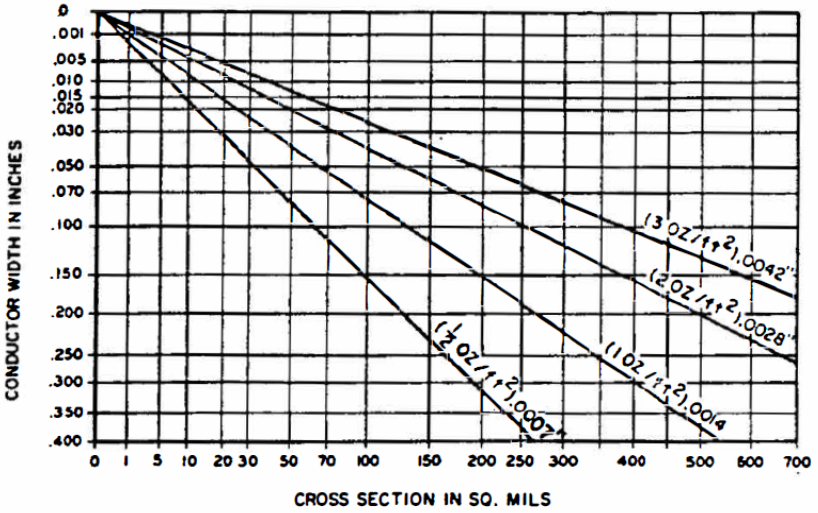


Figure B Conductor width to cross-section relationship

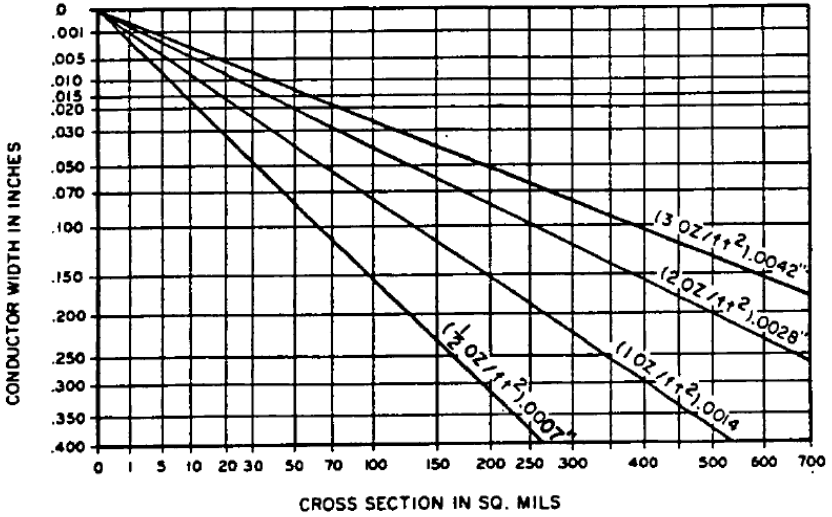


Figure B Conductor width to cross-section relationship

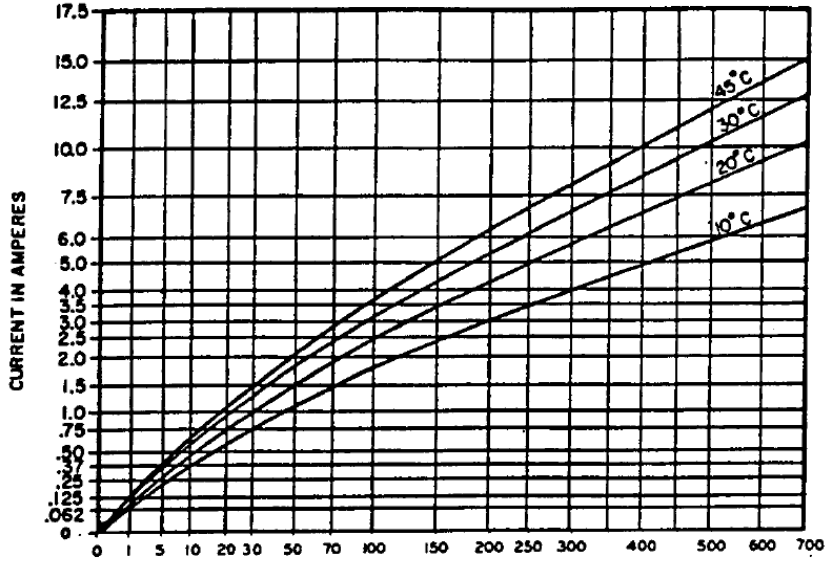
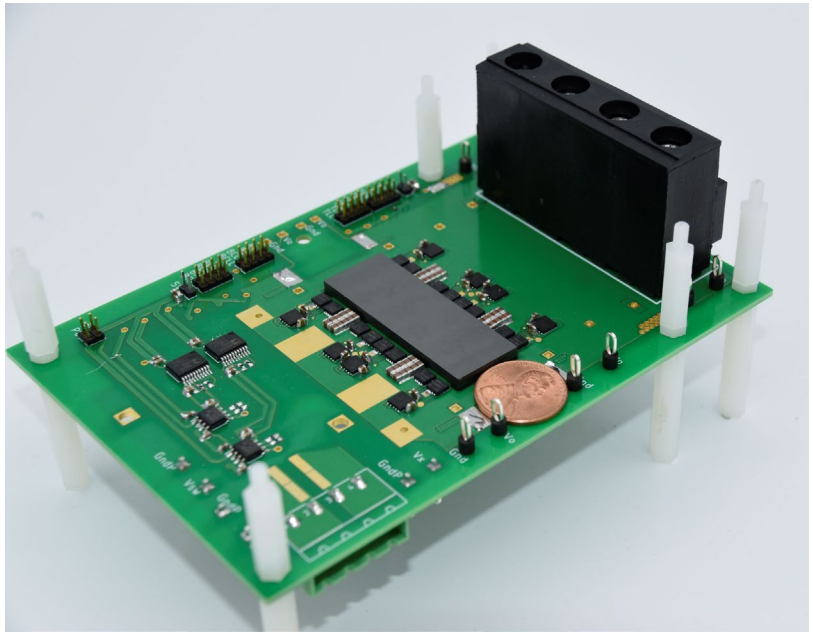


Figure C Internal Conductors

Other ways to estimate temperature rise

- When needed / available, more sophisticated estimates can be made using FEM tools (e.g., ANSYS Icepak)
- Still, guideline estimates are very valuable



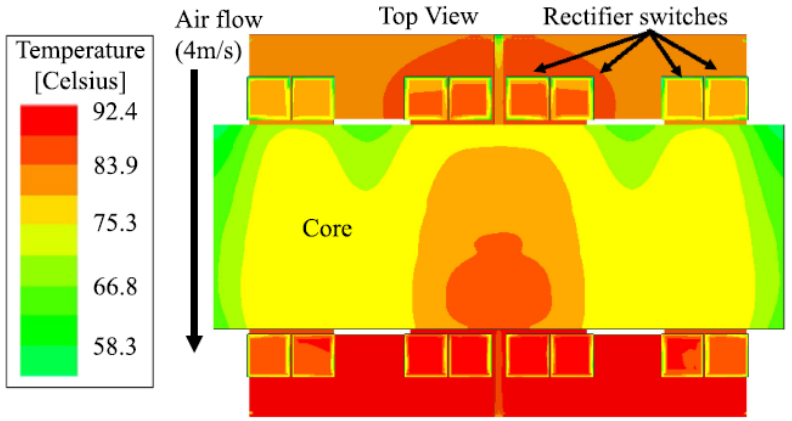


Fig. 8. ANSYS Icepak thermal simulation of the transformer.

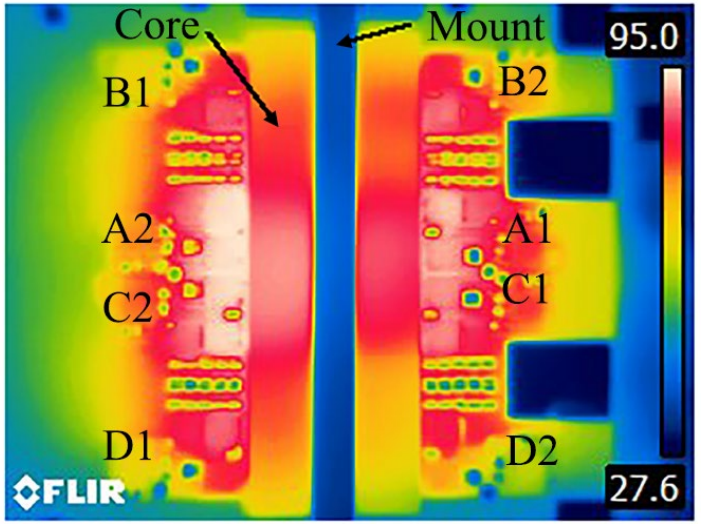


Fig. 13. Thermal image of secondary-side under full-load (obtained after 15 min of continuous operation, 22 °C room temperature). The fan is located to the right of the PCB.

Example from M.K. Ranjram and D.J. Perreault, "380-12 V, 1 kW, 1 MHz Converter Using Split-Phase, Fractional-Turn Planar Transformer," IEEE Transactions on Power Electronics, Feb. 2022.

Increasing current carrying

- To carry still higher currents:
- Can use PCB-mount busbars (aka “pcb stiffeners”) or mounted wires
- Can use PCBs with “extreme” plated copper

https://www.epectec.com/articles/heavy-copper-pcb-design.html

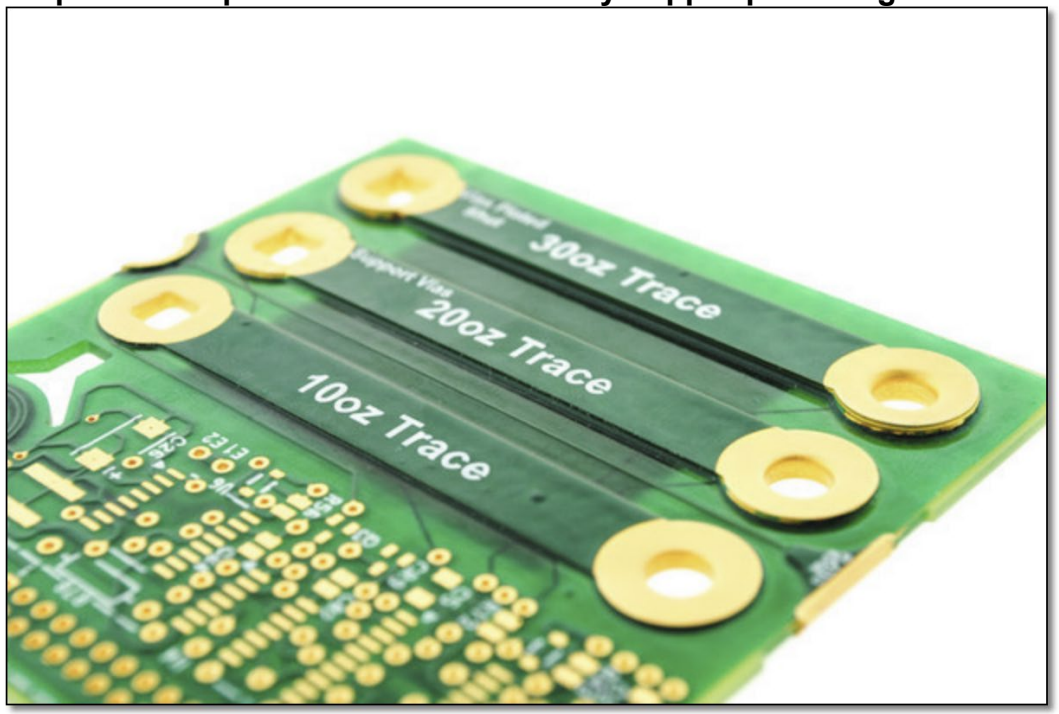


Figure 1. Sample featuring 2oz, 10oz, 20oz, and 30oz copper features on the same layer.

AC vs DC currents: Skin Depth

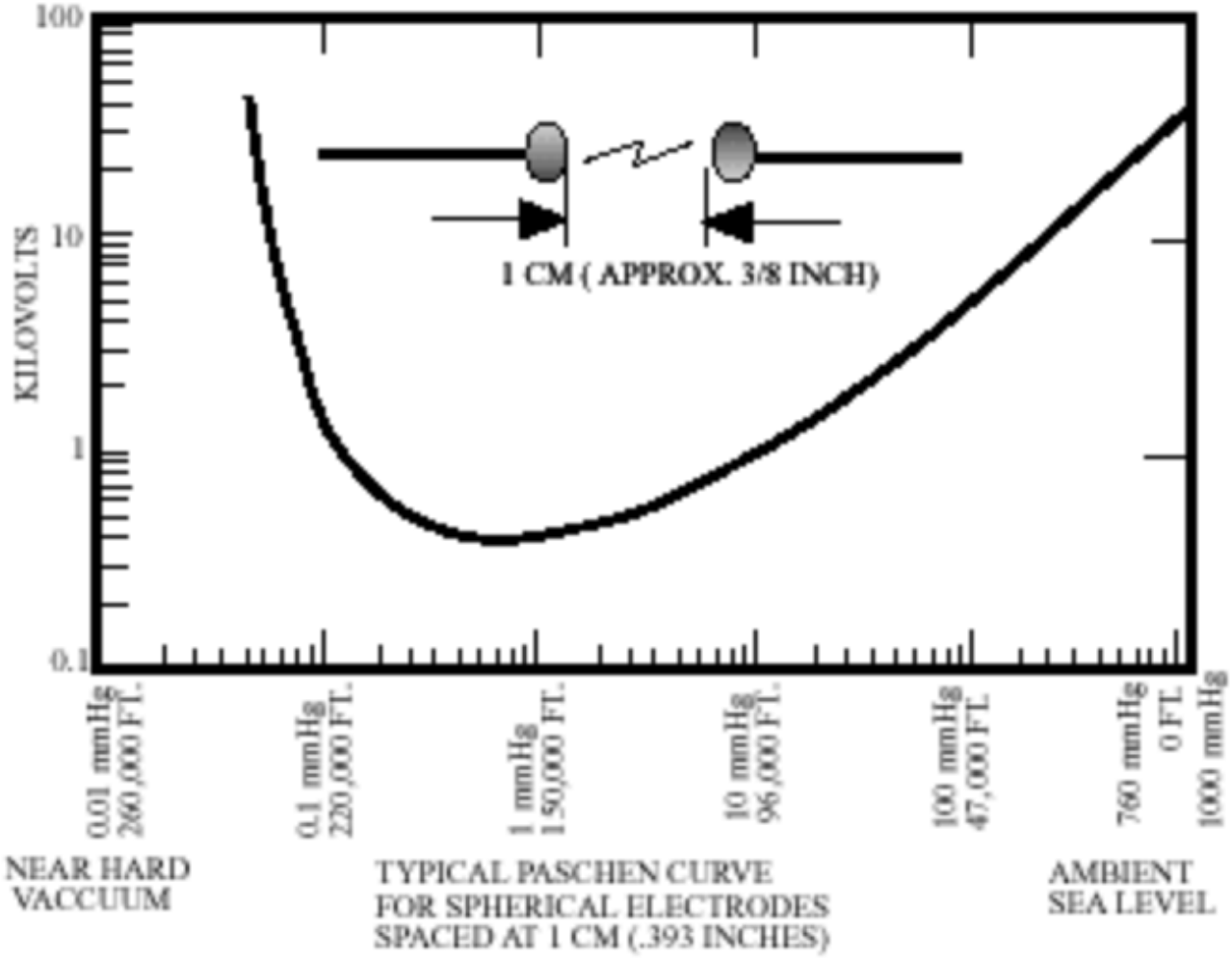
- **Prior estimates are for low-frequency rms currents (e.g., dc). High-frequency ac currents can cause higher loss owing to "skin effect"**
  - **Current only carried within 1 skin depth of surface**
    - **Cu skin depth ~ 21 μm at 10 MHz, 25 ° C**
  - **Orientation of return path is important for current distribution, loss**

$$\delta \triangleq \sqrt{\frac{\rho_{Cu}}{\pi \mu_{Cu} f}} = \frac{k}{\sqrt{f}}$$

@ 100°C in copper
$k \sim 7.5$ cm
@ 60 Hz $\delta \sim 0.97$ cm

Voltage Considerations

- Voltages on high-voltage nodes and traces set requirements on conductor spacing and layer spacing
- Guidelines are provided in various sources (IPC2221A, MIL-STD-275E)
- Limitations depend upon board material, layer, coating of board, elevation
  - Function of elevation because breakdown of air depends upon pressure
  - Paschen Curve: Breakdown voltage between metal plates in a gas vs. pressure (Friedrich Paschen, 1889)
  - Especially important for aerospace



https://catalog.teledynereynolds.com/Asset/1431.html

Conductor Spacing Table from IPC2221A

Table 6-1 Electrical Conductor Spacing

Voltage Between Conductors (DC or AC Peaks)	Minimum Spacing						
	Bare Board				Assembly		
	B1	B2	B3	B4	A5	A6	A7
0-15	0.05 mm [0.00197 in]	0.1 mm [0.0039 in]	0.1 mm [0.0039 in]	0.05 mm [0.00197 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]
16-30	0.05 mm [0.00197 in]	0.1 mm [0.0039 in]	0.1 mm [0.0039 in]	0.05 mm [0.00197 in]	0.13 mm [0.00512 in]	0.25 mm [0.00984 in]	0.13 mm [0.00512 in]
31-50	0.1 mm [0.0039 in]	0.6 mm [0.024 in]	0.6 mm [0.024 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.4 mm [0.016 in]	0.13 mm [0.00512 in]
51-100	0.1 mm [0.0039 in]	0.6 mm [0.024 in]	1.5 mm [0.0591 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.5 mm [0.020 in]	0.13 mm [0.00512 in]
101-150	0.2 mm [0.0079 in]	0.6 mm [0.024 in]	3.2 mm [0.126 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
151-170	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	3.2 mm [0.126 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
171-250	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	6.4 mm [0.252 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
251-300	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	12.5 mm [0.4921 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.8 mm [0.031 in]
301-500	0.25 mm [0.00984 in]	2.5 mm [0.0984 in]	12.5 mm [0.4921 in]	0.8 mm [0.031 in]	0.8 mm [0.031 in]	1.5 mm [0.0591 in]	0.8 mm [0.031 in]
> 500 See para. 6.3 for calc.	0.0025 mm /volt	0.005 mm /volt	0.025 mm /volt	0.00305 mm /volt	0.00305 mm /volt	0.00305 mm /volt	0.00305 mm /volt

Additional spacing per volt above 500 V spacing

B1 - Internal Conductors
B2 - External Conductors, uncoated, sea level to 3050 m [10,007 feet]
B3 - External Conductors, uncoated, over 3050 m [10,007 feet]
B4 - External Conductors, with permanent polymer coating (any elevation)
A5 - External Conductors, with conformal coating over assembly (any elevation)
A6 - External Component lead/termination, uncoated, sea level to 3050 m [10,007 feet]
A7 - External Component lead termination, with conformal coating (any elevation)

PCB Materials

- Can have breakdown straight through boards (for high voltages)
- Different PCB materials have different properties
  - Typical FR4, limit to 150 V/mil
  - Surface cover
    - Typical UV solder mask, 500 V/mil for ~0.7-1.5 mil thickness (aged)
    - Kapton can provide >2000 V/mil (aged)

Figure 11: Materials Supported in Multilayer High Voltage

Material Type	Max. Operating Temperature (°C)	T/G °C	Voltage (V/mil) Note 1	Aged rating (V/mil)	W°C/m
FR4	**105-130**	**160**	**800**	**300/150**	**0.21**
FR4 Hi-Temp.	**130-150**	**170**	**800**	**300/150**	**0.22**
BT Epoxy	**140-160**	**180**	**1300**	**600/400**	**0.40**
Polyimide	**150-190**	**200**	**900**	**700/500**	**0.25**
HVPF*	**180-200**	**210**	**3000 to 7000**	**3000/2000**	**0.28**

***HVPF is a trademark of Sierra proto express.**

R. Tarzwell & K. Bahl, "High Voltage Printed Circuit Design & Manufacturing Notebook," Sierra Proto Express

PCB Materials

- Improved electrical insulation of board and components is sometimes achieved by additional coatings (e.g., “corona dope”) or “potting” of the board/components

PCB Element Shapes

- Corona is induced by electric field
  - Corona is partial breakdown, but can carbonize board and lead to runaway failure
  - For high v, avoid conductor shapes with sharp corners that concentrate electric field

Figure 13: Picture of corona

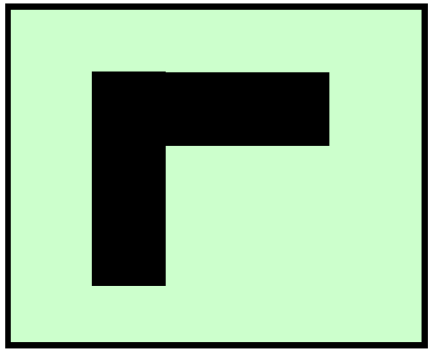


Figure 1: Bad corner design

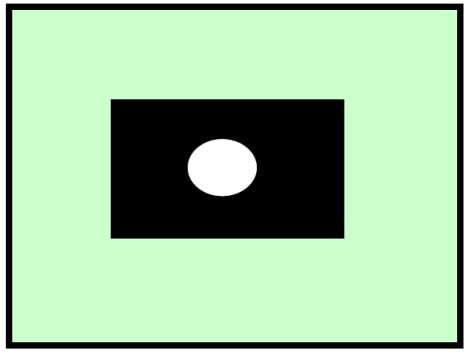


Figure 2: Bad pad design

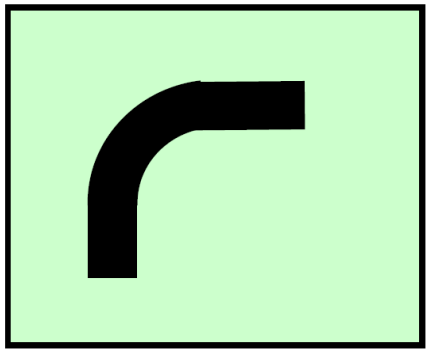


Figure 3: Good corner design

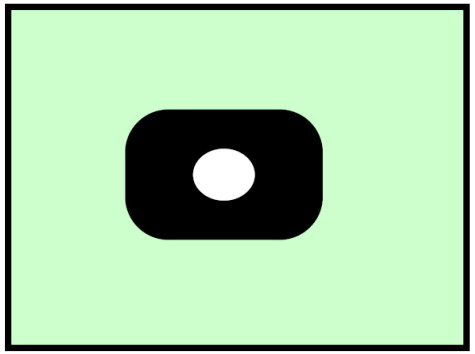
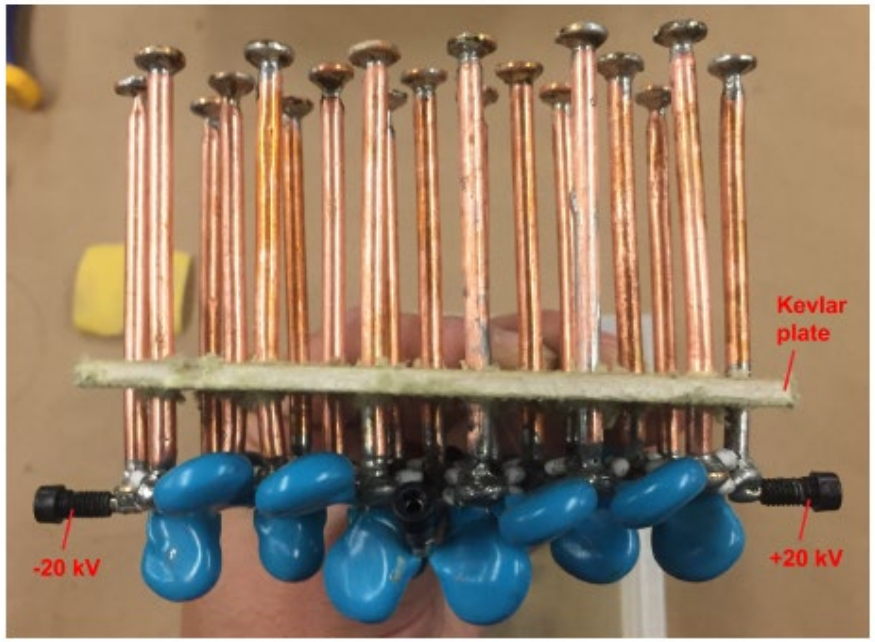


Figure 4: Good pad design

R. Tarzwell & K. Bahl, "High Voltage Printed Circuit Design & Manufacturing Notebook," Sierra Proto Express

PCB Element Shapes

- Corona is induced by electric field
  - Corona is partial breakdown, but can carbonize board and lead to runaway failure
  - For high v, avoid conductor shapes with sharp corners that concentrate electric field
  - Applies to components/structures too!
    - 40 kV voltage multiplier rectifier for a resonant dc/dc converter



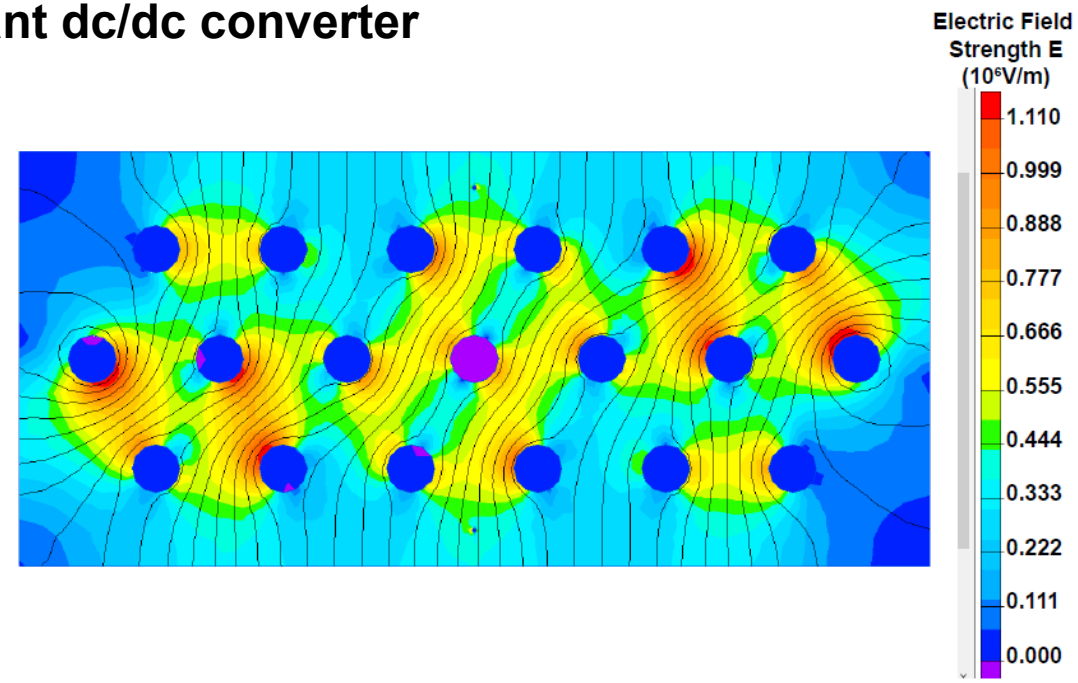
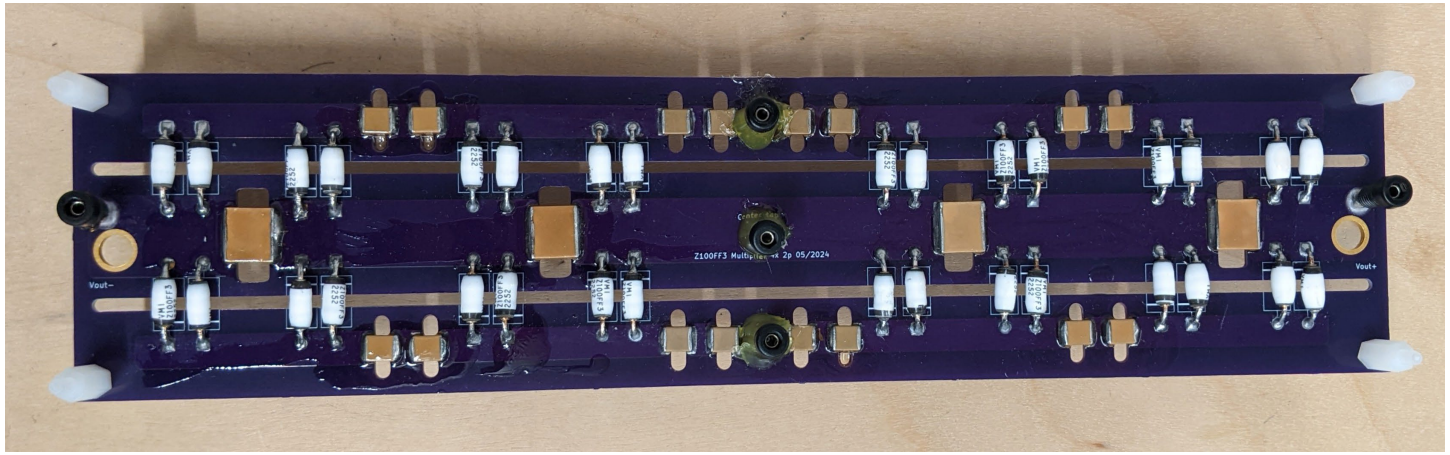


Figure 2-13: An example electric-field simulation of the voltage multiplier structure (each diode blocks 7.5 kV and the heat sink diameter is 3/16").

Y. He "Towards Lightweight High Voltage Power Conversion", MIT PhD Thesis, Feb. 2020

PCB Element Shapes

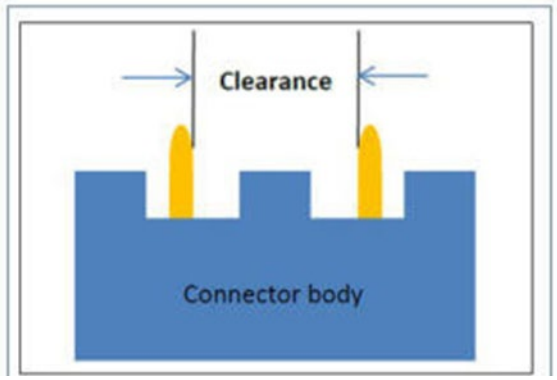
- Can prevent carbonization runaway by inserting slots in board between high-voltage terminals
  - Also can be used to prevent “tracking” along board if contaminants are present

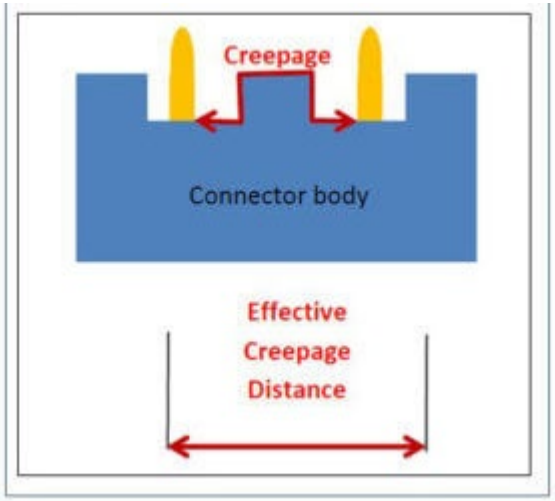


Mihir Shevgaonkar, Voltage Multiplier Rectifier, MIT 2024

Clearance vs. Creepage

- Some specifications (e.g., UL 60950-1, for safety of IT equipment) specify design rules that include both clearance and creepage
  - Clearance is “shortest air distance” between two elements/traces
  - Creepage is “distance along surface/board” between elements
- Clearance relates to direct breakdown through air, but creepage can be important for “tracking” along surface that can lead to breakdown
  - Board slots and/or insulating inserts can help increase creepage distance





https://blog.samtec.com/post/creepage-and-clearance-and-why-we-care-about-it/

Dielectric Loss in PCBs

- For combinations of high voltage, high frequency, board dielectric loss can also be a concern
  - Microwave circuits, but also at lower frequencies, higher voltages

$$\tan\delta = \frac{\mathrm{ESR}}{|X_c|} = \omega C \cdot \mathrm{ESR} = \frac{\sigma}{\varepsilon'\omega}$$

  - Loss tangent is fraction of ac capacitive stored energy lost in each ac cycle
    - Tan(δ)=1/Q of board capacitance
  - Compute to estimate whether undue loss or heating will occur

Material	Tg	e_r*	Tan (f)	DBV (V/mil)	WA, %
Rogers RO 4350	280	3.48	0.0037	780	0.04
Standard FR-4 Epoxy Glass	125C	4.1	0.02	1100	0.14
Multifunctional FR-4	145C	4.1	0.022	1050	0.13
Tetra Functional FR-4	150C	4.1	0.022	1050	0.13
Nelco N4000-6 Hi Tg FR-4	170C	4	0.012	1300	0.10
GETEK	180C	4.1	0.011	1100	0.12
BT Epoxy Glass	185C	4.1	0.023	1350	0.20
Nelco 4000-13SI	210	3.25	0.009	1400	0.09
Cyanate Ester	245C	4	0.01	800	0.70
Polyimide Glass	285C	4.1	0.015	1200	0.43
Teflon	N/A	2.2	0.0002	450	0.01
		* Measured with a TDR using velocity method.			
		Resin content 55%			

Tg = glass transition temperature
er = relative dielectric constant
Tan (f) = loss tangent
DBV = dielectric breakdown voltage
WA = water absorption

All materials with woven glass reinforcement except Teflon.
Note: Teflon is not a multilayer PCB material.

https://resources.altium.com/p/increasingly-important-role-loss-tangents-pcb-laminates

Half-Bridge Layout – Bottom-Side Device Cooling

E. Persson, "Optimizing PCB Layout for HV GaN Power Transistors," IEEE Power Electronics Magazine, June 2023.

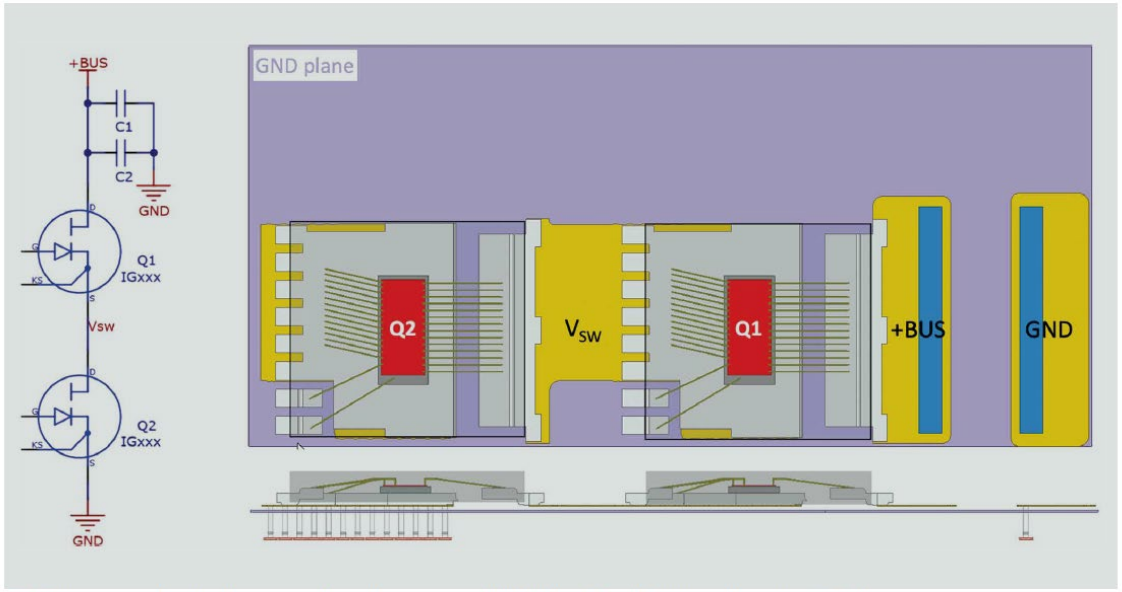


FIG 5 Low power-loop inductance using surface-mounted "TOLL"-packaged GaN transistors. L = 2.8 nH.

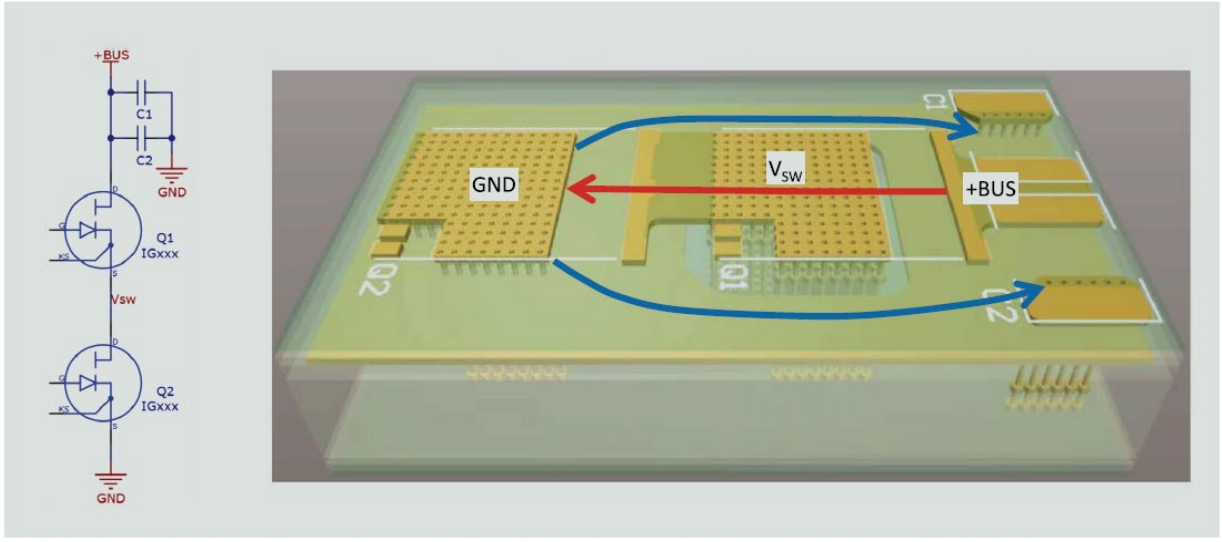


FIG 8 Double-sided return-path around thermal via field helps to minimize lateral-loop inductance. L = 6.2 nH.

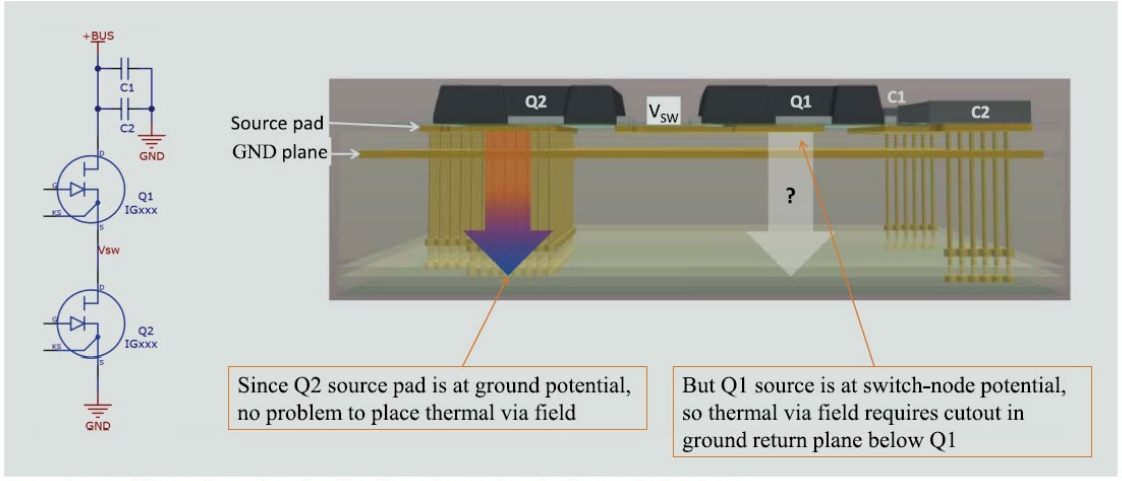


FIG 6 The need for Q1 thermal path will make optimum electrical layout challenging.

Parameters of interest : θ_{JA}, θ_{JC}, θ_{CA}, θ_{JT} **From TI AN2020**

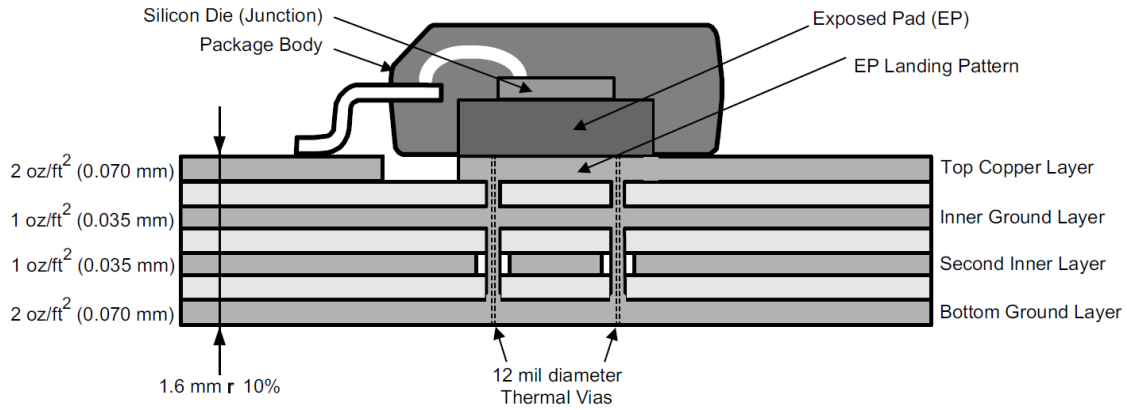


Figure 1. IC Mounted On A Four-Layer Printed Circuit Board

Half-Bridge Layout – Top-Side Device Cooling

E. Persson, “Optimizing PCB Layout for HV GaN Power Transistors,” IEEE Power Electronics Magazine, June 2023.

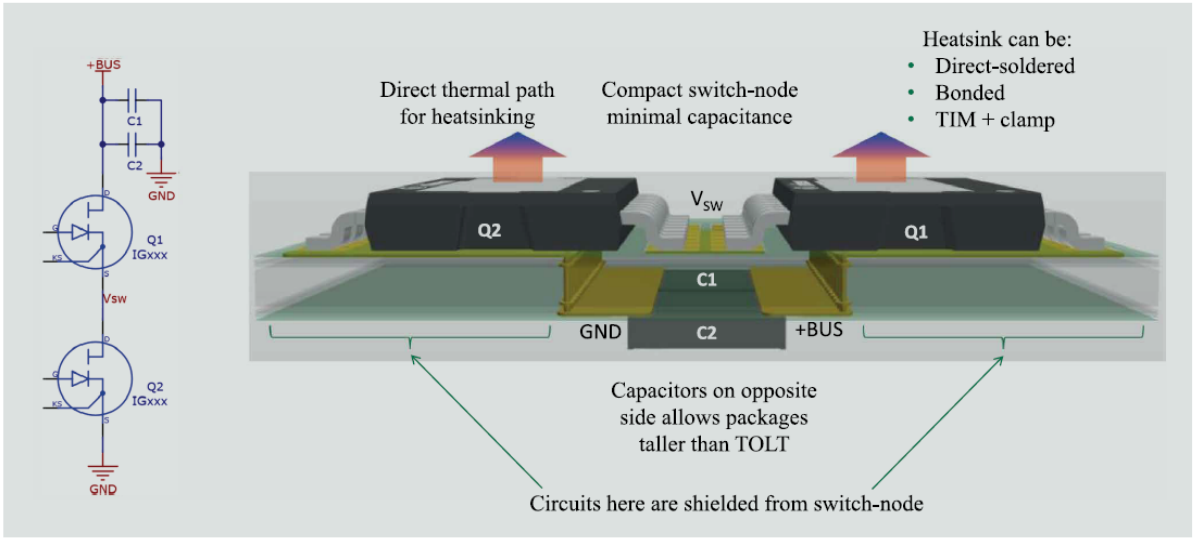


FIG 9 Topside-cooled transistors enable optimization of both electrical and thermal paths results in 5.8 nH loop inductance.

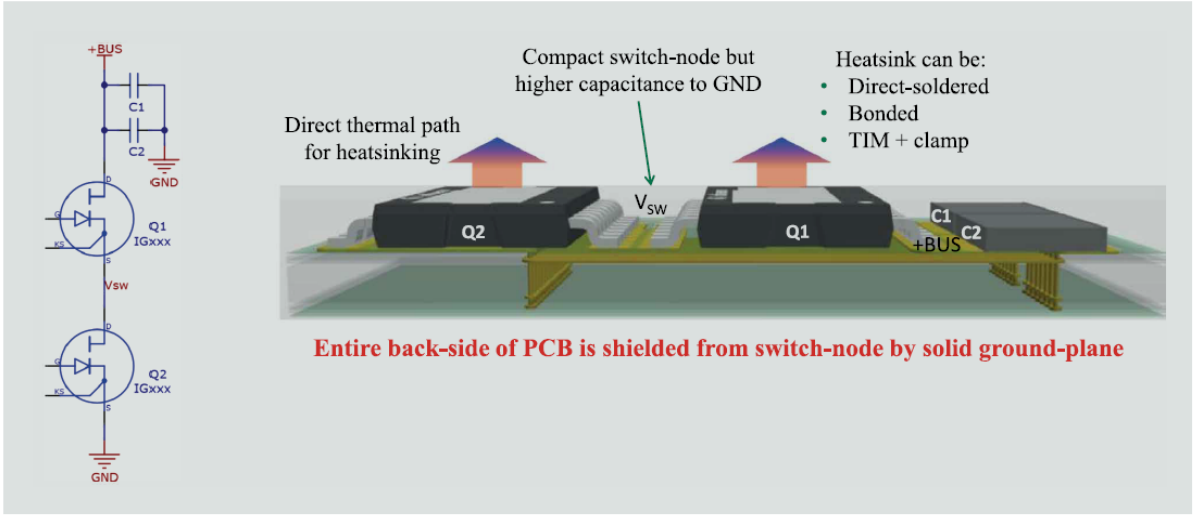


FIG 10 Moving capacitors to same side as transistors for lowest overall inductance provides 4.9 nH loop inductance.tance.

Thermal Resistance Modeling – Through-PCB Heat Xfer

- See Texas Instruments AN2020 for calculation details
  - Heat sink often mounted to PCB bottom
- Heat transfer coefficient from surface of PCB to ambient air often ROUGHLY estimated as 10 W/m^2-k
  - Also see thermal modeling in Kassakian, et. al. “Principles of Power Electronics” Cambridge University Press, 2023

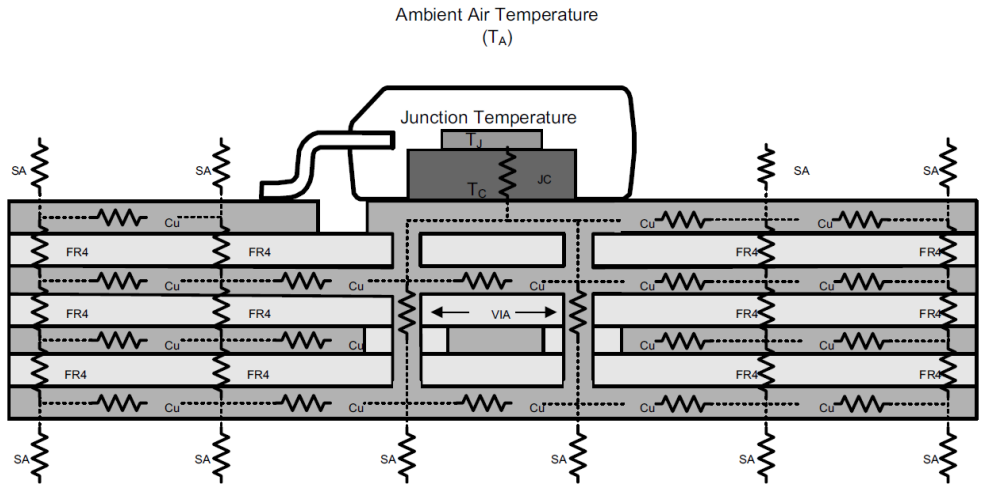


Figure 3. Expanded Thermal Resistance Model For A Typical PCB

Table 1. Typical Thermal Resistance Values

Name	Value	Description	Conditions	Equation
θ_{Cu}	71.4 °C / W	Lateral thermal resistance of copper plane.	Length = 1 cm, width = 1 cm, 1 ounce copper thickness = 0.0035 cm, thermal conductivity of copper (λ_{Cu}) = 4 W / (cm °C)	$\theta_{Cu} = \frac{\frac{1}{\lambda_{Cu}} \times \text{Length}}{\text{Area}} = \frac{0.25 \frac{°C\ cm}{W} \times 1\ cm}{1\ cm \times .0035\ cm}$ (2)
θ_{VIA}	261 °C / W	Thermal resistance of typical 12 mil via.	Via length = 0.165 cm (65 mils), 0.5 ounce copper plating thickness = 0.00175 cm, drill hole radius = 6 mil (0.01524 cm), thermal conductivity of copper (λ_{Cu}) = 4 W / (cm °C)	$\theta_{VIA} = \frac{\frac{1}{\lambda_{Cu}} \times \text{Length}}{\text{Area}} = \frac{0.25 \frac{°C\ cm}{W} \times 0.165\ cm}{\pi \times [(0.01524\ cm)^2 - (0.01524\ cm - 0.00175\ cm)^2]}$ (3)
θ_{SA}	1000 °C / W	Thermal resistance from the surface of a 1 cm square of the PCB to the ambient air due to natural convection.	1 cm square, a first order approximation of the heat transfer coefficient of PCB Board to Air for natural convection is (h) = 0.001 W / (cm^2 °C)	$\theta_{SA} = \frac{\frac{1}{h}}{\text{Surface Area}} = \frac{1000 \frac{°C\ cm^2}{W}}{1\ cm \times 1\ cm}$ (4)
θ_{FR4}	13.9 °C / W	Vertical thermal resistance of FR-4 substrate.	1 cm square, FR-4 thickness = 0. 032 cm (12.6 mil), thermal conductivity of FR-4 (λ_{FR4}) = 0.0023 W / (cm °C)	$\theta_{FR4} = \frac{\frac{1}{\lambda_{FR4}} \times \text{Thickness}}{\text{Area}} = \frac{435 \frac{°C\ cm}{W} \times 0.032\ cm}{1\ cm \times 1\ cm}$ (5)