THE ART AND SCIENCE OF PCB DESIGN

IAP 2025

Lecture - 06 PCB LAYOUT

PCB Layout 2/2

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Outline

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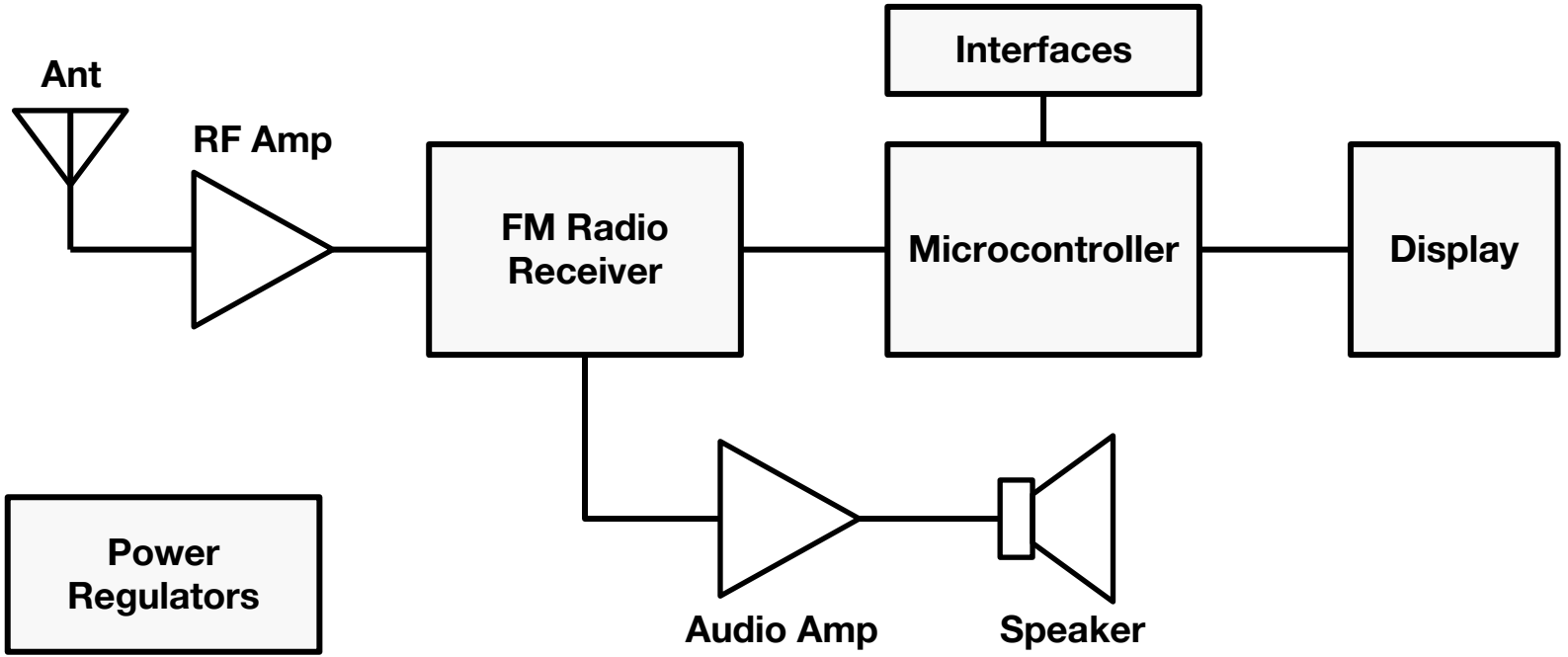
- Review
- Routing and Placement Considerations
  - Traces
  - Integrated Circuits
  - Board
  - Interfaces
- Examples

Schematic

Block Diagram



System Design

Course Project

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Identify Problem ✓

Devise Solution ✓

Identify System Parameters ✓

Create/Model System ✓

Design PCB!

FM radio receiver

Course Project!

Later topics

Fabrication → Test/Debug

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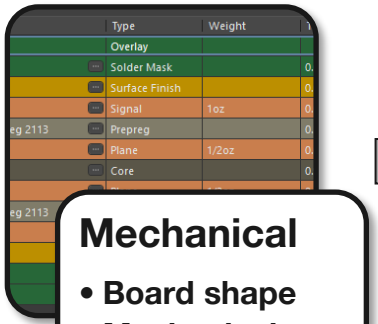
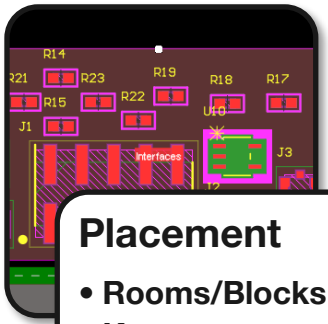
Basic PCB Layout

Design Flow



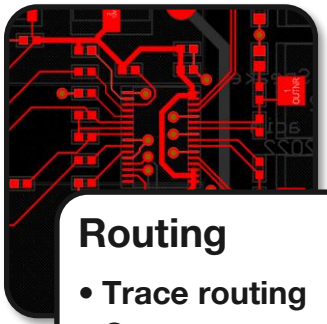
Mechanical

- Board shape
- Mechanical Features
- Stackup



Placement

- Rooms/Blocks
- Keep-out zones
- Individual component arrangement



Routing

- Trace routing
- Copper pours

Verification

- DRC Report
- Simulation

Repeat as needed

PCB Construction

Putting it all Together

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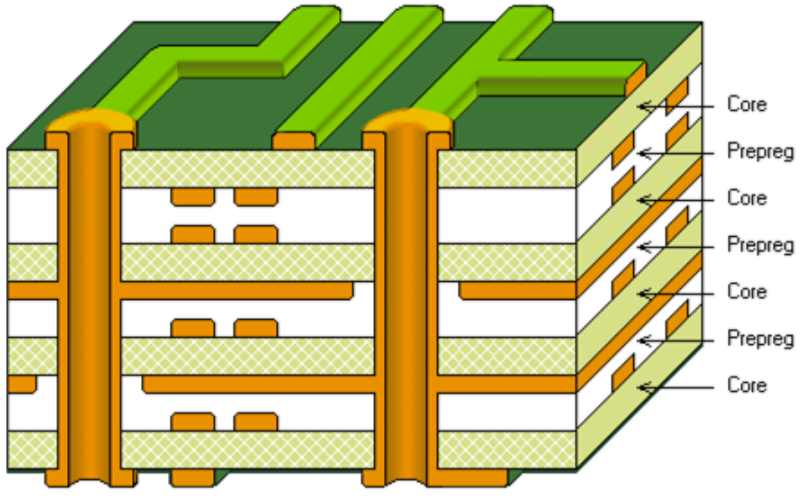
Substrates and their copper laminates can be stacked together to create multilayer PCBs, with layers connected to another using vias.

- **Typically 2-20 conductive layers**
- **The non-conductive substrates are known as dielectrics which can range in materials depending on the application**
- **Soldermask/surface finish/silkscreen on top and bottom**



https://morepcb.com/8-layer-pcb-stack-up/

Basic PCB Layout

Routing

Red – Top Layer
Blue – Bottom Layer
Yellow - Silkscreen

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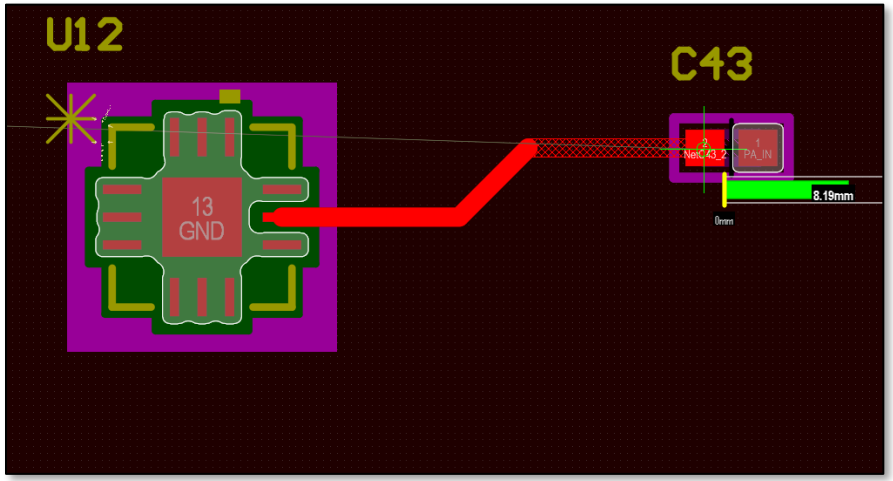

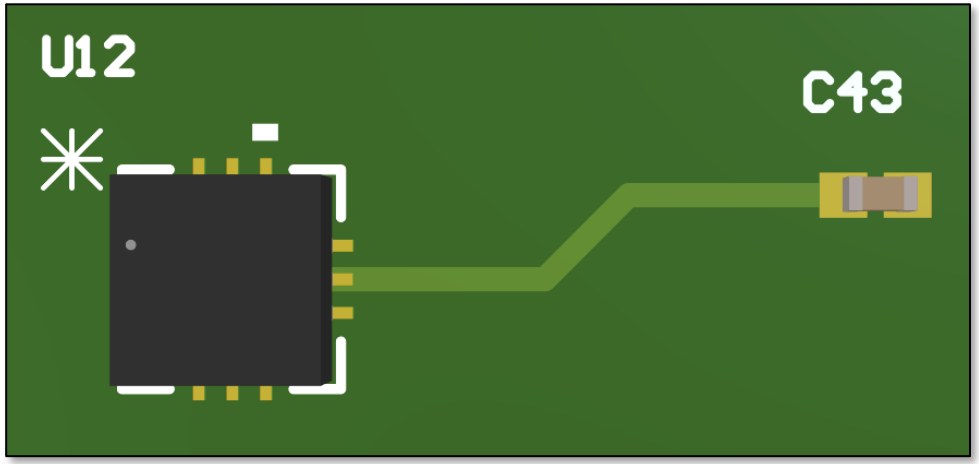

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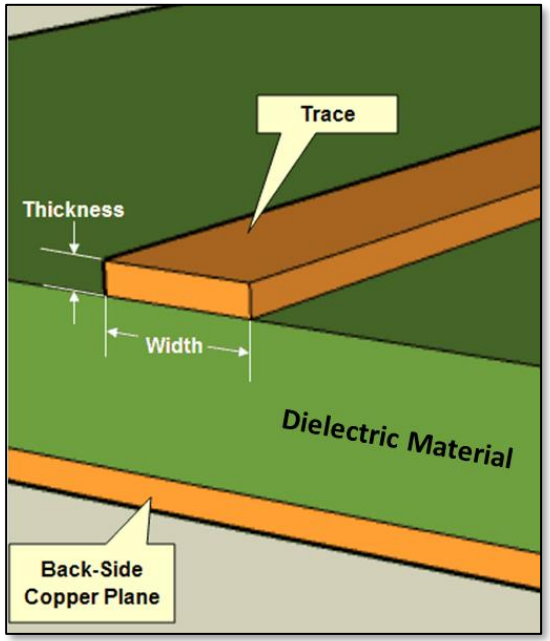
Routing Traces

Trace width and length



Recall that bulk resistance in a conductor is:

$$R = \frac{L}{\sigma A}$$

Trace cross section (width and thickness) determines current-carrying capability and resulting temperature rise (keep < 10^0C rise, see IPC-2152)

- **Use polygon pours in place of traces for high current nets (increases conductor cross section)**
- **Keep traces as short as possible to avoid voltage drops and signal distortions**

https://www.protoexpress.com/blog/trace-current-capacity-pcb-design/

Routing Traces

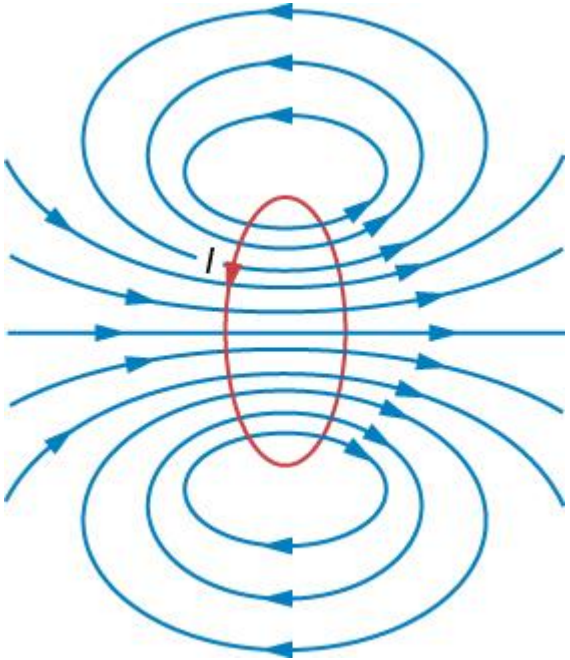
Trace Path

Recall Faraday's Law of Magnetic Induction:

$$\vec{\nabla} \times \vec{E} = -\frac{\partial \vec{B}}{\partial t}$$

Changing magnetic flux results in an electric field circulation (curl) → current

- **For long traces, avoid creating loops to prevent capture of external magnetic flux**
- **Avoid long traces with no termination – forms an antenna at high frequencies**



Routing Traces

Trace Spacing

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PCB fabricators have limits on how close they can manufacture two adjacent traces. These clearance minimums must be met to avoid tolerance errors

- **For high voltage traces, electric breakdown in the dielectric or air can cause shorts, proper spacing is required**
- **Keep high frequency and noisy traces separate from other traces. Fields generated by these can induce currents in other traces (think Ampere-Maxwell)**

Copper Specifications

Spec	Value
Copper Layers	2
Copper Weight	1oz
Trace Spacing	6mil (0.1524mm)
Trace Width	6mil (0.1524mm)
Annular Ring	5mil (0.127mm)
Board Edge Keepout	15mil (0.381) from nominal board edge
Via Plating Thickness	1mil (0.0254mm)

$$\vec{\nabla} \times \vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t}$$

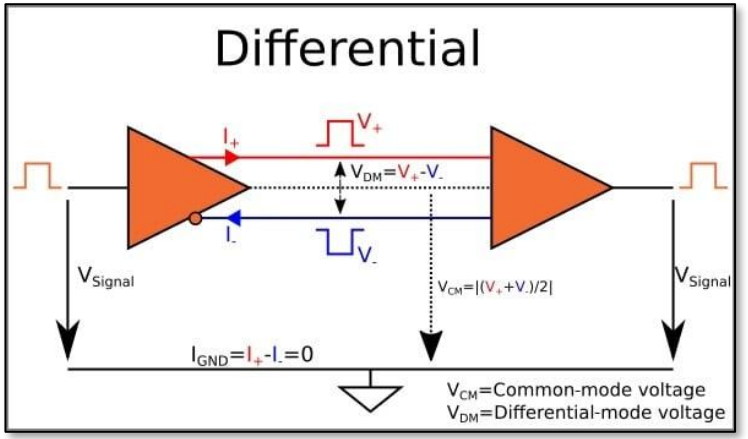
Routing Traces

Trace Spacing

High frequency (RF and high-speed digital) traces often have special routing requirements that govern trace width and clearance, typically to maintain a particular impedance throughout

- **Differential traces consist of two of such traces with the additional requirement of needing to be routed next to and symmetric to each other as well as having the same length**

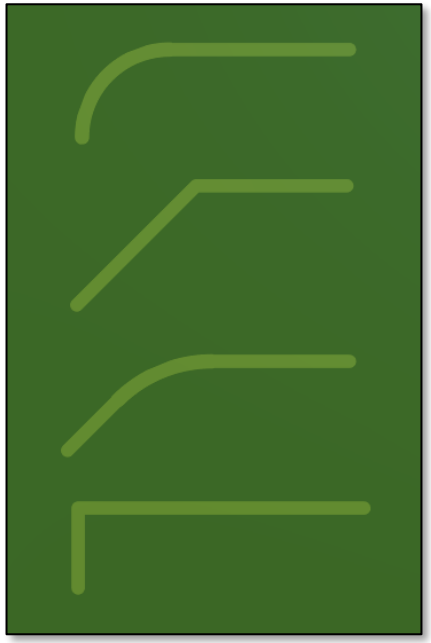
- **Differential traces have improved common-mode noise immunity over single-ended traces**



https://www.allaboutcircuits.com/technical-articles/the-why-and-how-of-differential-signaling/

Routing Traces

Trace Shape

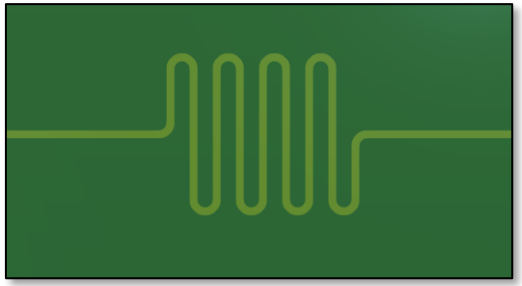


Good for sharp turns with high frequency signals

Commonly seen on many boards, often preferred for low frequency signals

Best for high frequency signals

Fine for low frequency applications, should generally avoid



Lengthening trace to improve digital timing

Removes fringing capacitance

Chamfered corner for impedance matching

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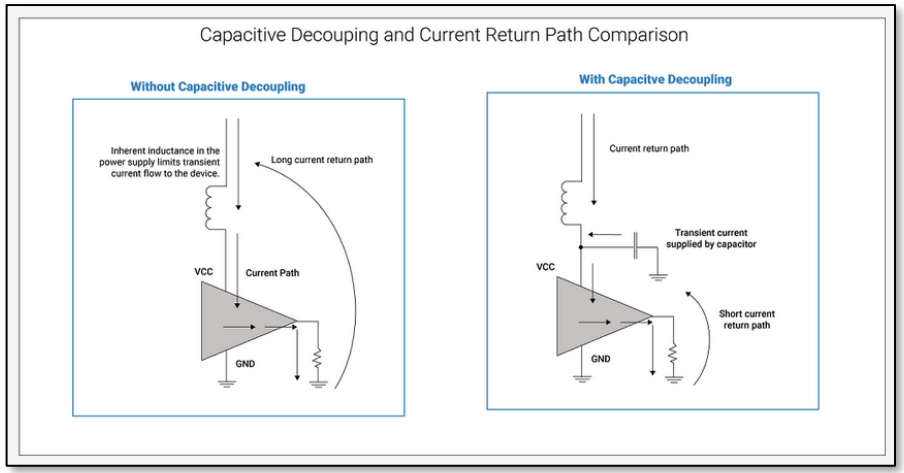
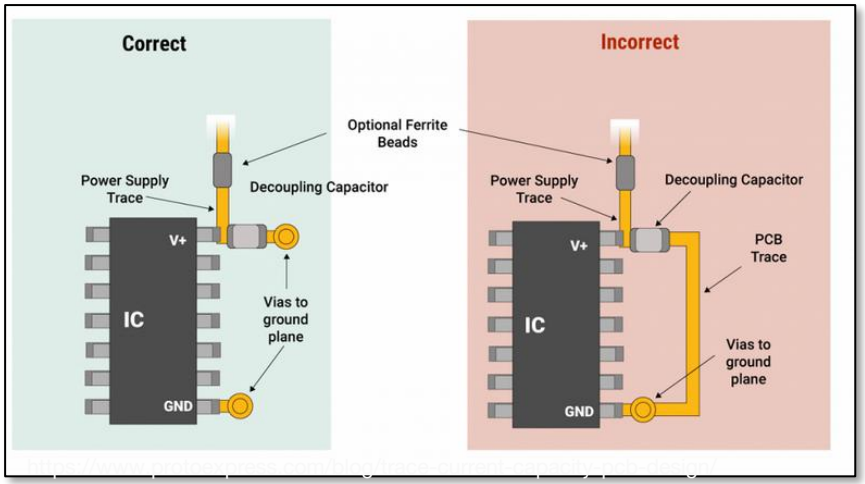
Placing Integrated Circuits

Decoupling





Decoupling capacitors are placed near the power input pins of ICs and provide filtering of noise and transients

- **Typically, a large- and small-valued capacitor combination is used as close to the IC as possible. (e.g. 100 nF and 200 pF)**

Placing Integrated Circuits

Thermal Reliefs

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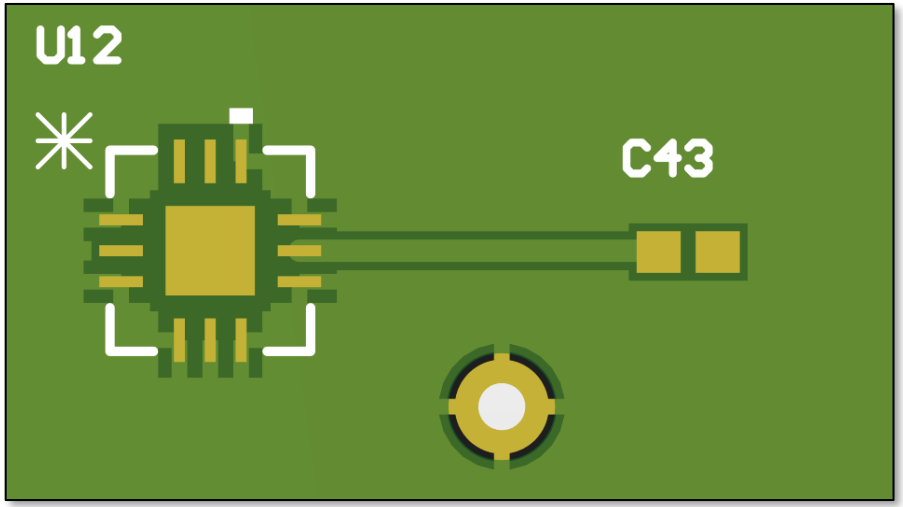
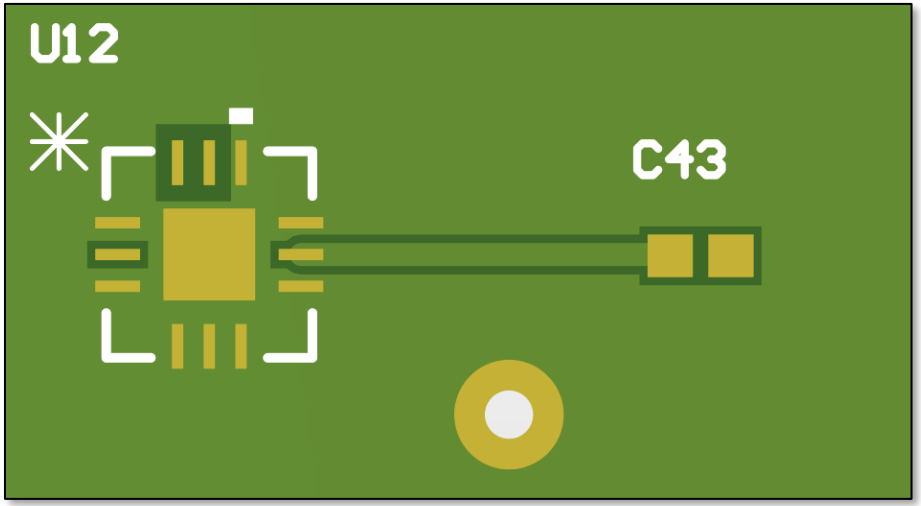


With thermal reliefs



Without thermal reliefs

Thermal reliefs improve hand solderability but increases impedance for return path connection

Basic PCB Layout

Copper Pours

Red – Top Layer
Blue – Bottom Layer
Yellow - Silkscreen

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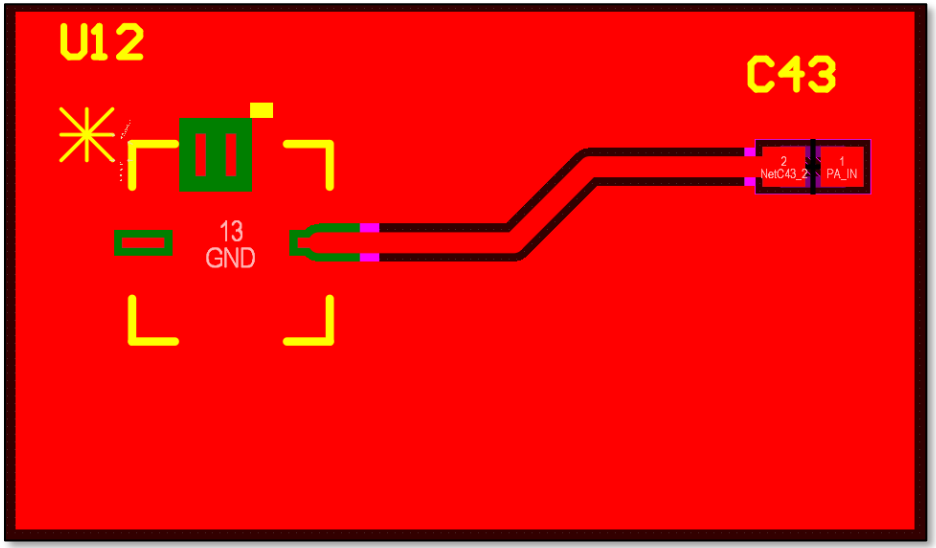

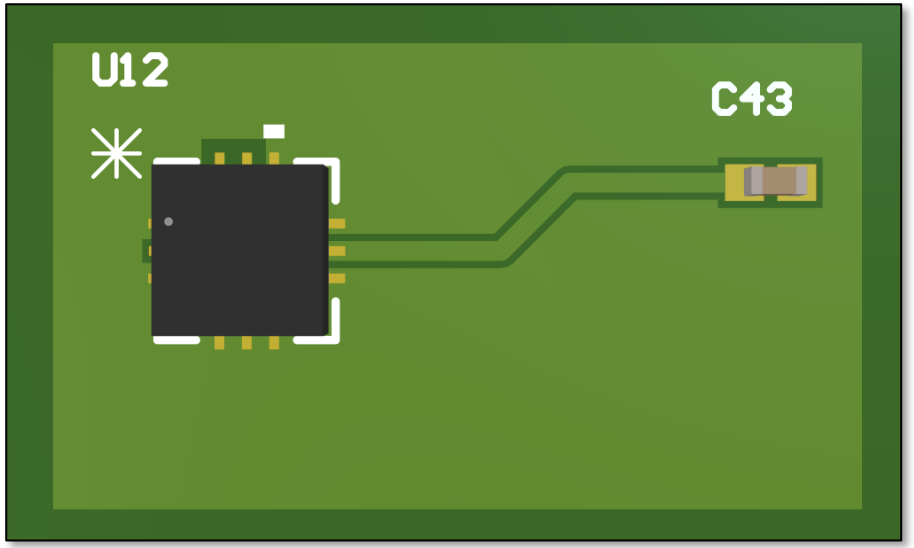

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Board Configuration

Power Planes

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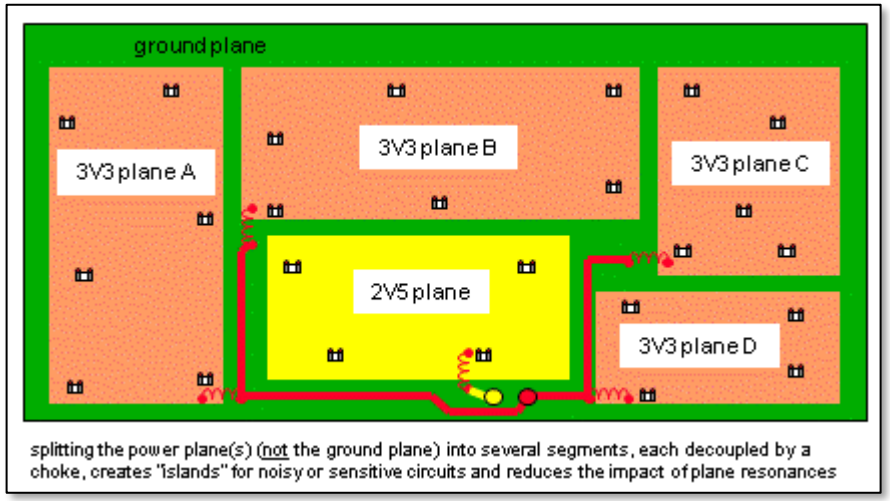
In a multilayer board, parts of or entire internal layers can be assigned to specific power nets to form a power plane

Vias can be used for devices (typically on the top or bottom layers) to easily access a power net

- **Reduces number of traces**
- **Limits power losses**
- **Isolates noisy power nets**



splitting the power plane(s) (not the ground plane) into several segments, each decoupled by a choke, creates "islands" for noisy or sensitive circuits and reduces the impact of plane resonances

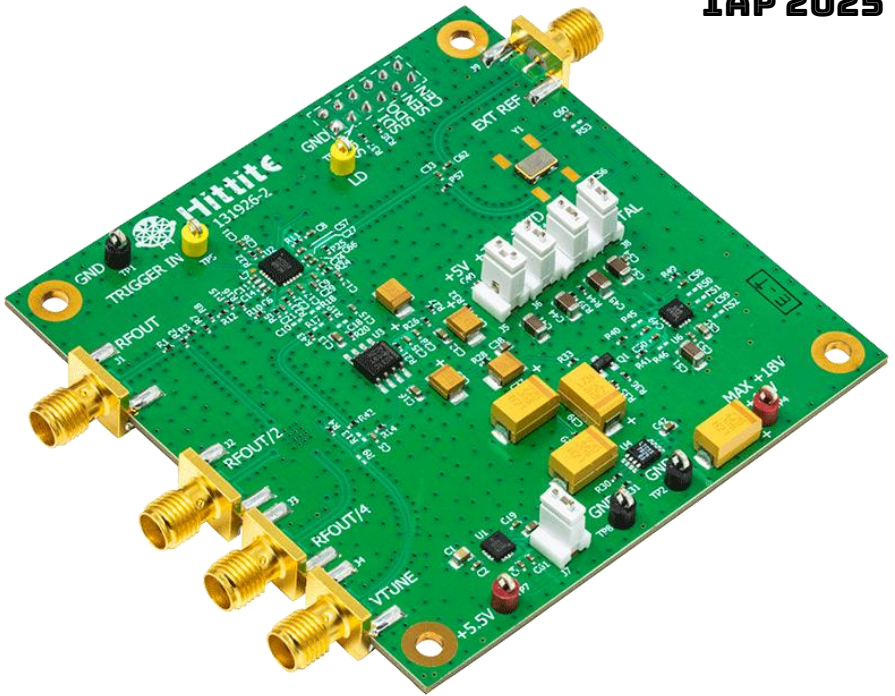
http://www.elmac.co.uk/EMC_SelfStudy-std/Index.htm?context=380

Board Configuration

Ground Pours

Like power planes, entire layers should be dedicated to the ground net to create a low-impedance return path

- **Empty regions should be filled with ground pours to further provide short return path and reduce fringing fields**
- **Ensure there are no copper ground islands**
- **Via stitching can help ensuring ground pours are connected well**



https://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boards-kits/EVAL-HMC703LP4E.html

Board Configuration

Discontinuous Ground Planes

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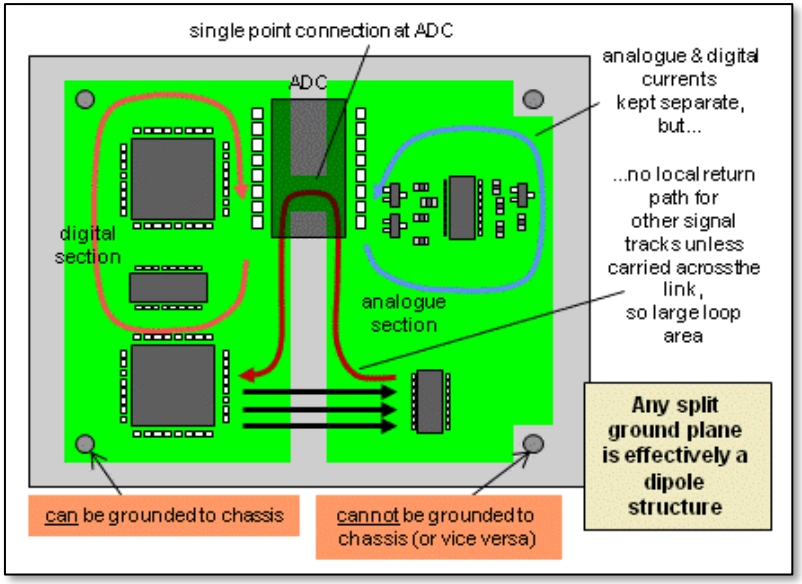
Sometimes we do want poorly connected ground planes

Common case: high-speed digital and high-frequency analog circuits located on the same board

- **Separate ground planes that are poorly connected to each other as well as careful placement, can isolate noise and prevent each from interfering with the other.**



http://www.elmac.co.uk/EMC_SelfStudy-std/Index.htm?context=380

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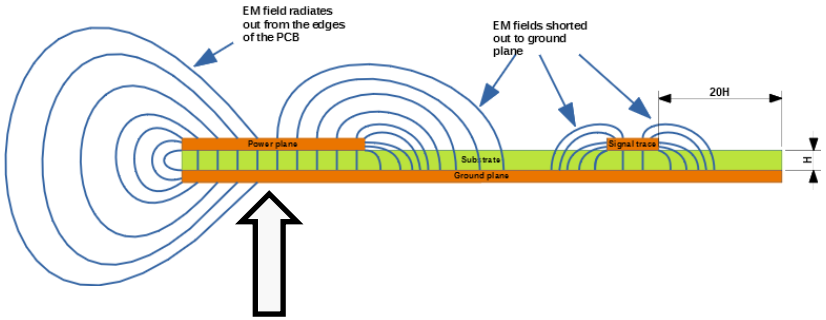
Board Configuration

Edge Effects

- **Planes and traces on parallel layers can form inductive loops and capacitors, which create fringing fields on the board edge**
- **Follow 10h rule: all planes and traces should be routed at least a distance of ten times the height of the substrate layer from board edge to avoid effects from fringing fields**
- **Often manufacturers will have a board edge constraint anyways**



Top and bottom copper also forms inductive loop that can capture magnetic flux near the edge

https://easyeda.com/forum/topic/The-20H-and-Ground-Plane-Extension-rules-benefits-and-limitations-of-applying-them-4d443d32240545aeb9fa9516d2fdac3f

Board Configuration

Shielding

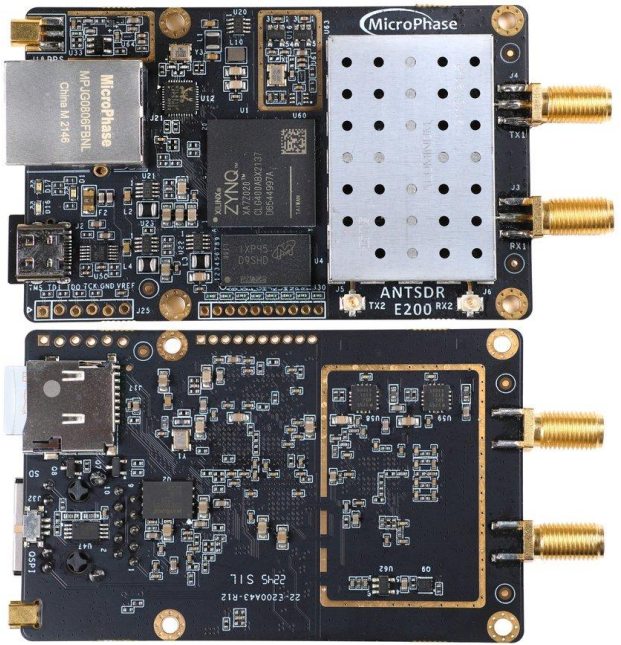
Metal shielding around sensitive components can prevent external fields from interfering (particularly electric fields)

$$\vec{\nabla} \cdot \vec{D} = \rho$$

- **Shields should have a generous connection to ground along its perimeter**

Highly permeable materials can be used to shield magnetic fields

- **Usually will be placed in the enclosure**



https://www.crowdsupply.com/microphase-technology/antsdr-e200

PCB Construction

Soldermask

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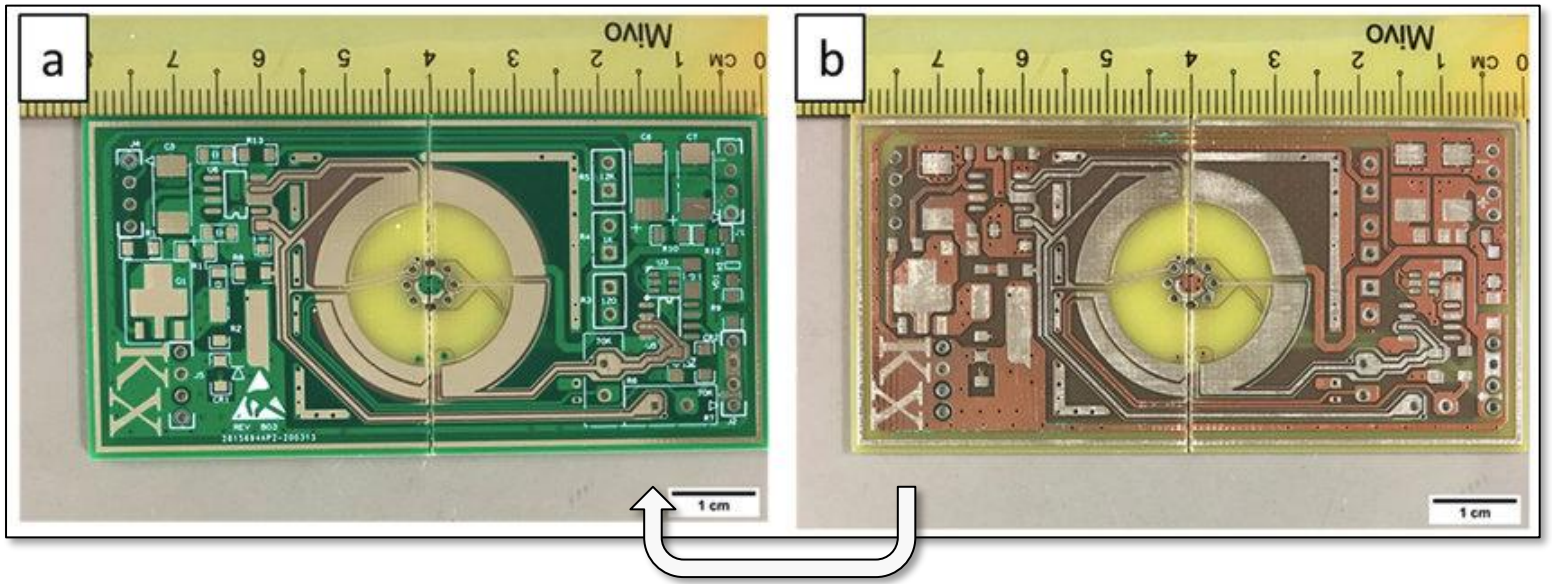
To protect the board during assembly and from corrosion, a non-conductive coating (soldermask) is applied to copper that is not to be soldered to



https://www.researchgate.net/figure/Coarse-PCB-pieces-a-before-the-removal-of-solder-mask-and-b-after-the-removal-of_fig7_355966696

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Board Configuration

Soldermask Removal

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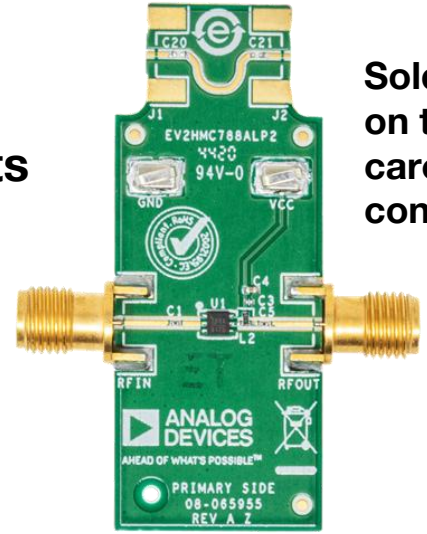
Soldermask, as a dielectric materi,al can create boundary conditions that produce unwanted effects for high frequency circuits

- **RF/microwave circuits will typically remove soldermask around traces to prevent this**
- **In high power applications, removing soldermask from high-current traces allows solder or a metal block to be attached to increase trace cross section and reduce resistance**



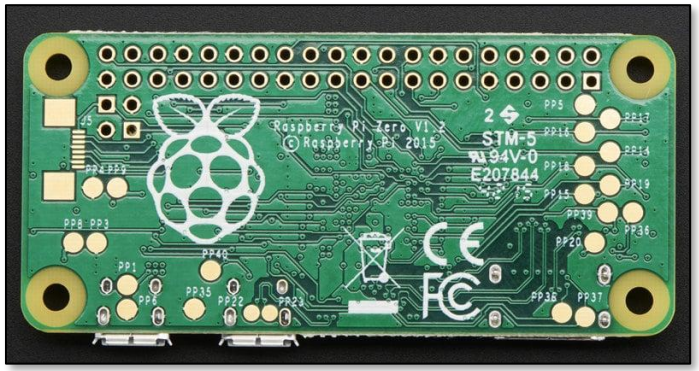
Soldermask is removed on traces that need to be carefully impedance controlled

https://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boards-kits/EVAL-HMC788ALP2.html

Interfaces

Test Points

- **Placed on nets where important debugging and test information can be gained**
- **High frequency circuits requires special care when placing test points as they can cause signal distortions**
- **Put many on your PCBs**



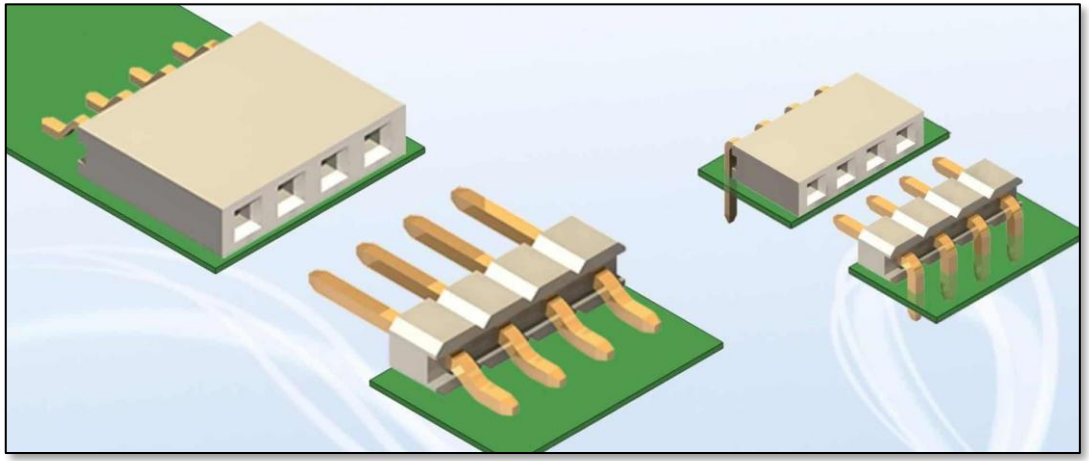
https://www.adafruit.com/product/3825

https://learn.adafruit.com/introducing-the-raspberry-pi-zero/a-tour-of-the-pi-zero

Interfaces

Connectors

- Connectors allow for external interfacing with a PCB
- Typically mounted on the PCB's edge
- SMT connectors can delaminate but do not introduce any protrusions on the bottom board side
- Use THT if possible



Both connectors are edge-mount, however the left one is SMT and the right one is THT

Summary

Key Takeaways

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- ❑ Segmentize your board: keep digital with digital and analog with analog to best extent you can prevent co-interference
- ❑ Ensure there are many debug points, PCBs often do not work first-try
- ❑ Layout circuits as compactly as possible while maintaining enough space to assemble and debug
- ❑ Use ground pours and ground/power planes
- ❑ Ensure trace sizing requirements are met for each net
- ❑ Choose connectors that are accessible, appropriate for the type of signal they will carry, and will have a strong mechanical connection to the board
- ❑ Ensure appropriate mounting points are present

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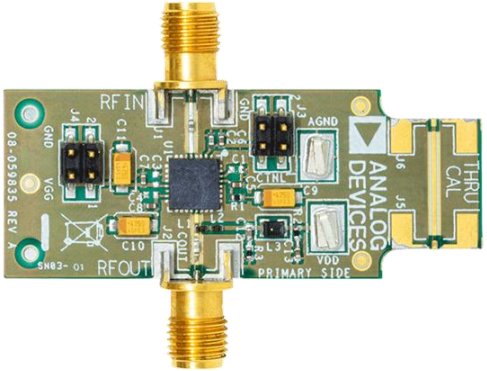
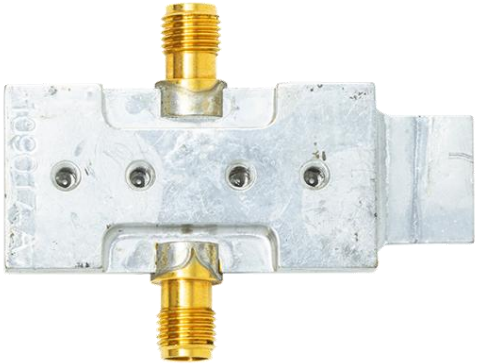
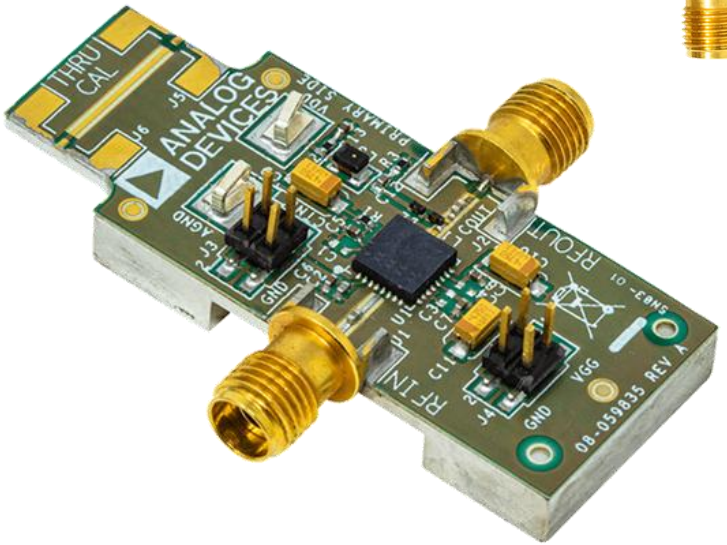
Examples

Examples

RF/Microwave







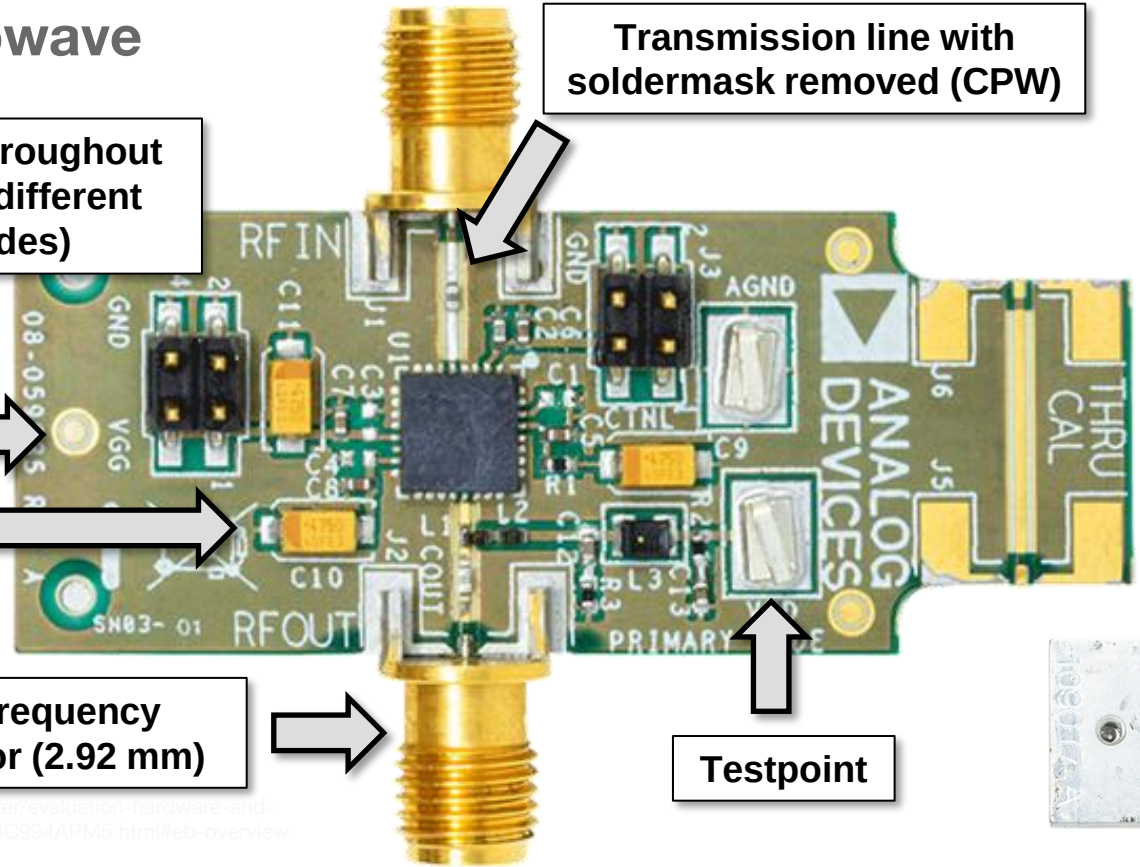
https://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boards-kits/EVAL-HMC994APM5.html#eb-overview

Evaluation board for a 28 GHz amplifier

- **Ground pour throughout, a metal block attached to the bottom to increase ground plane cross section**
- **Soldermask removed on RF-carrying traces**
- **Traces made as short as possible**
- **Many testpoints**
- **Connectors appropriately selected to handle high frequencies (2.92 mm connectors)**

Examples

RF/Microwave



Transmission line with soldermask removed (CPW)

Ground pour throughout board (notice different green shades)

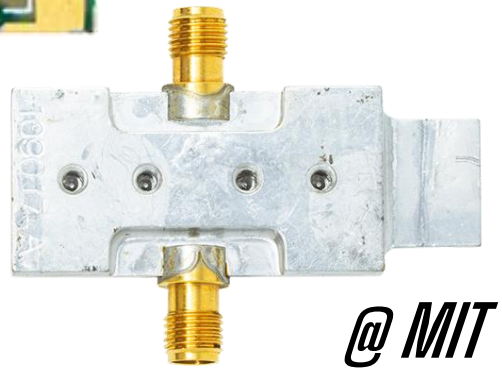
Testpoint

Decoupling Capacitor

High-frequency connector (2.92 mm)

Testpoint

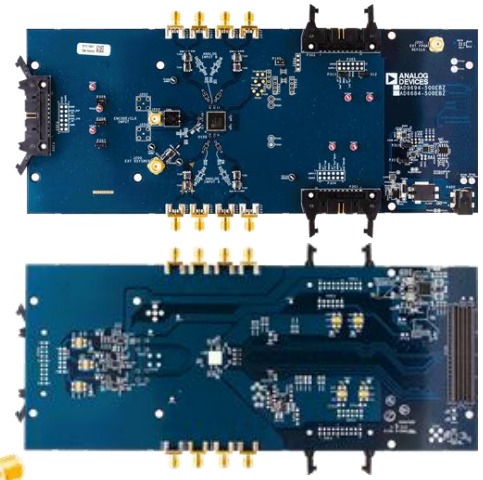
Metal block soldered to underside

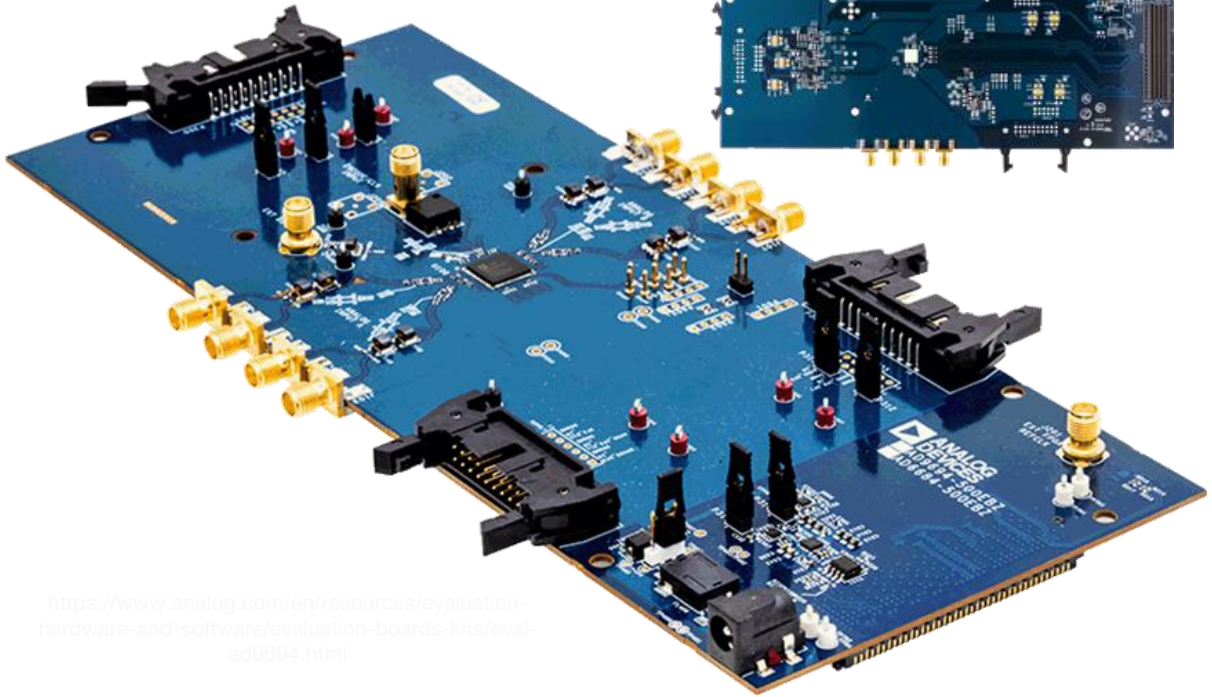


https://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boards-kits/EVAL-HMC994APM5.html#eb-overview

Examples

High-Speed Digital





https://www.analog.com/en/resources/evaluation-hardware-and-software/evaluation-boards-kits/eval-ad9694.html

135 MHz ADC Evaluation board

- Far seperated digital and analog sections
- Separate internal ground plane for digital section
- Differential signals are routed symmetrically
- Contains mounting holes
- Many debug and test points

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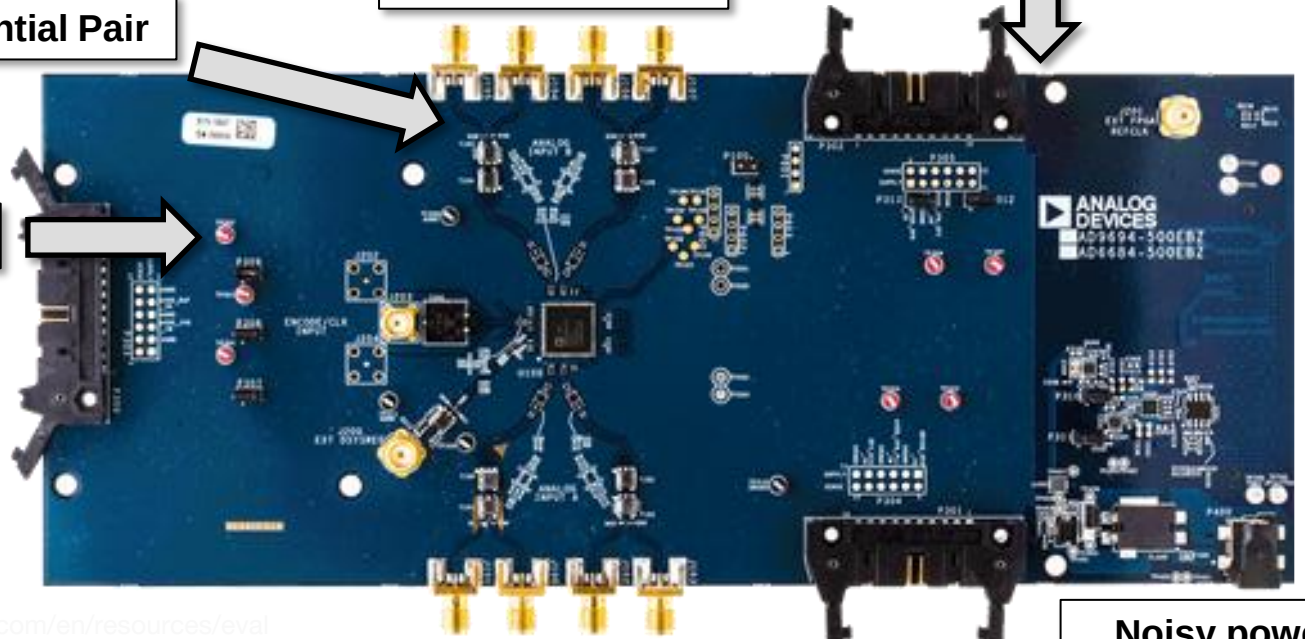
Examples

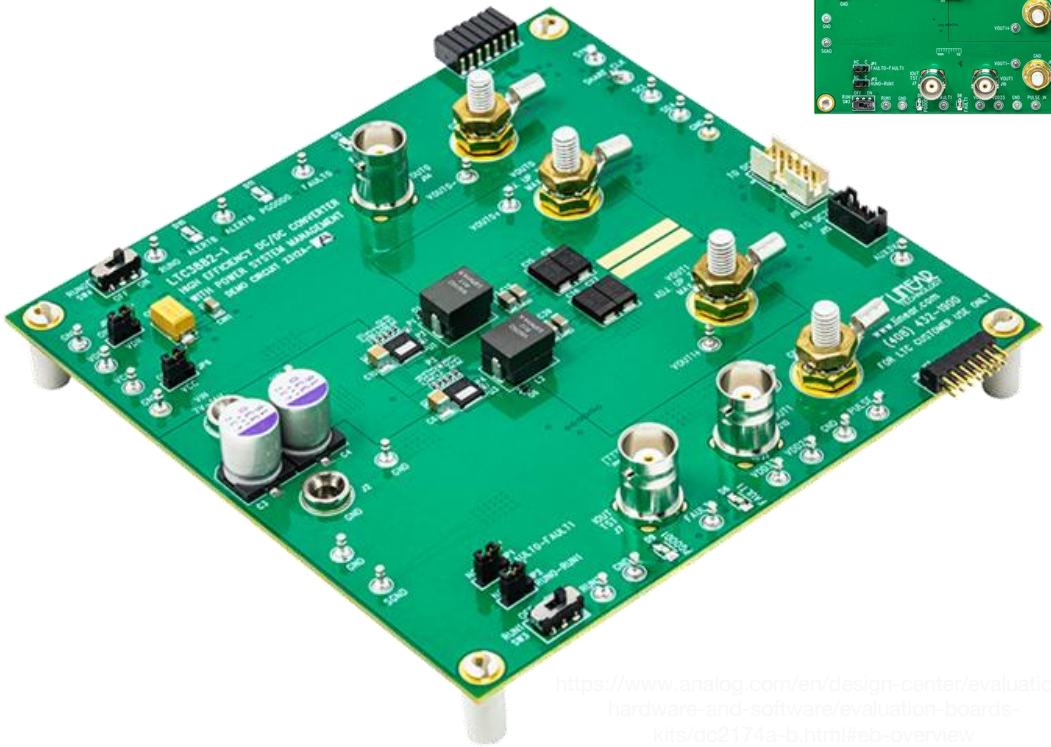
High-Speed Digital

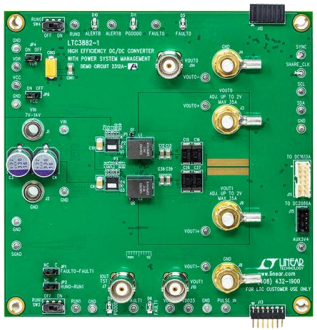


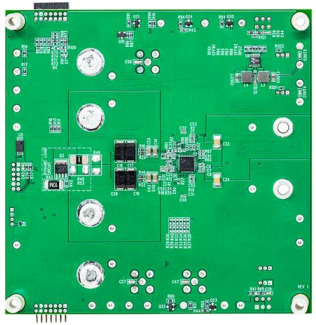
https://www.analog.com/en/resources/evaluation-hardware-and-software/evaluation-boards-kits/eval-ad9694.html

Examples

High Power







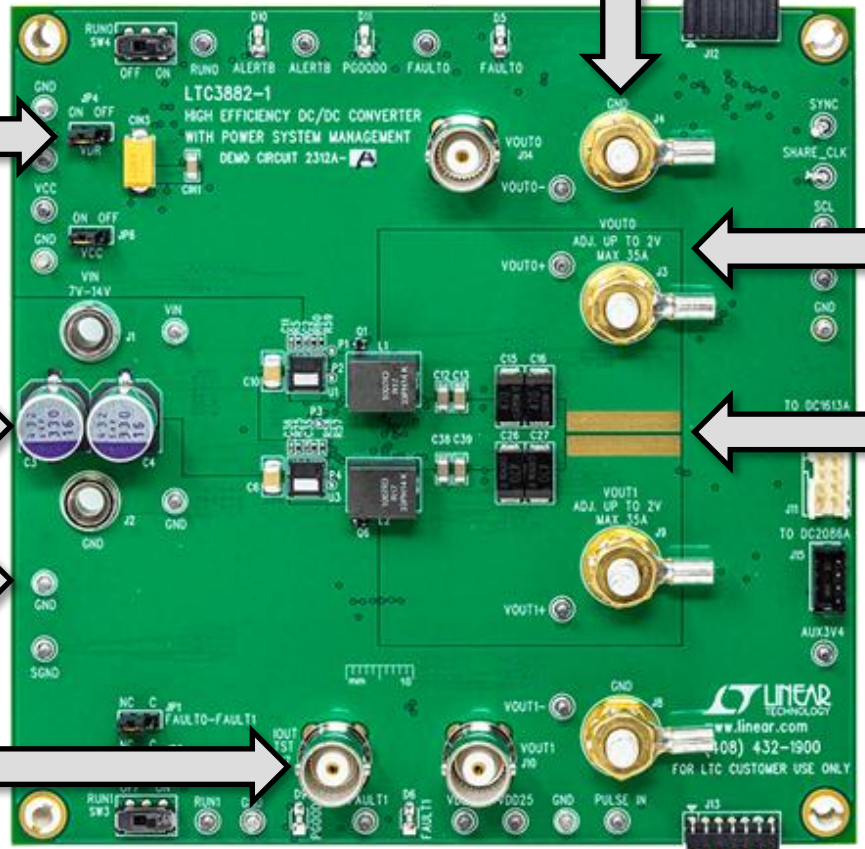
70 A Buck Converter Evaluation Board

- **Wide traces across layers for input and output with via stitches**
- **Appropriate high current crimped connections for output**
- **Additional connectors mounted along edge**
- **No thermal reliefs**

https://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boards-kits/dc2174a-b.html#eb-overview

Examples

High Power



High-power Connectors (ring)

Removable Jumper

Copper Pour for Output

Decoupling Capacitors

Removed Soldermask for Bridging Outputs

Testpoint

High-sensitivity Testpoints

Copper Ground Pour