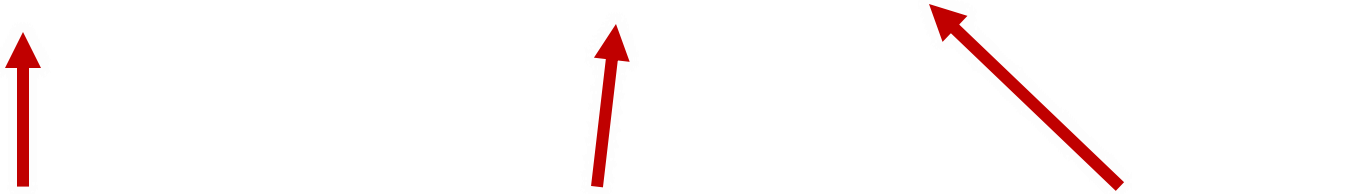
Advanced PCB Layout: **High Power**

Amanda Jackson

January 21, 2026

$$P = IV$$



High power

High current

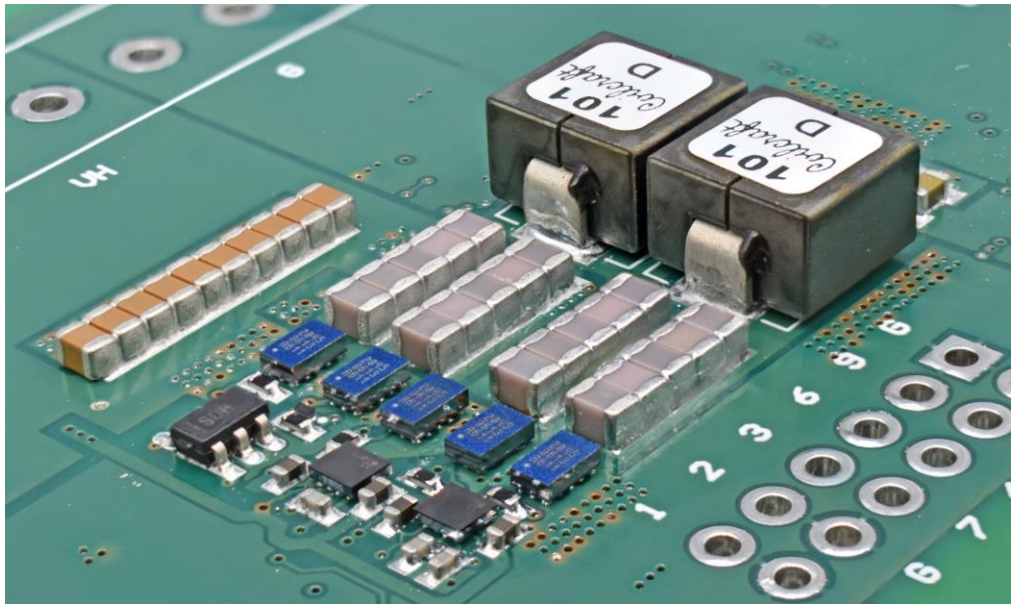
(and/or)

High voltage

Examples of high-power circuits

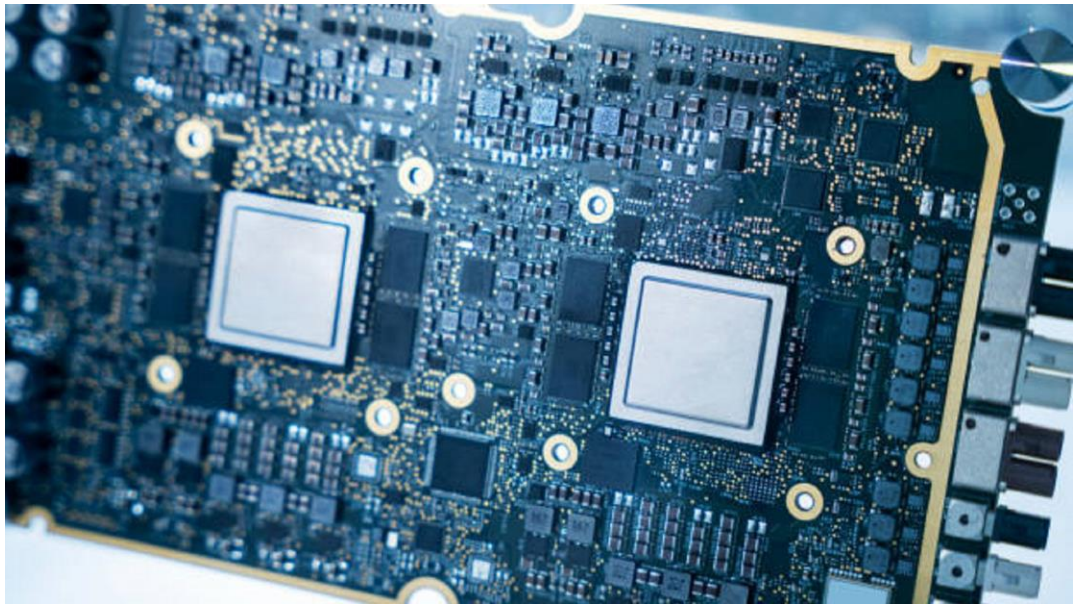
Power converters

- High voltage and/or high current



Computers

- Low voltage, high current



Our goal:

Don’t blow anything up!

High-Voltage Considerations

Nodes in a circuit are separated by insulators

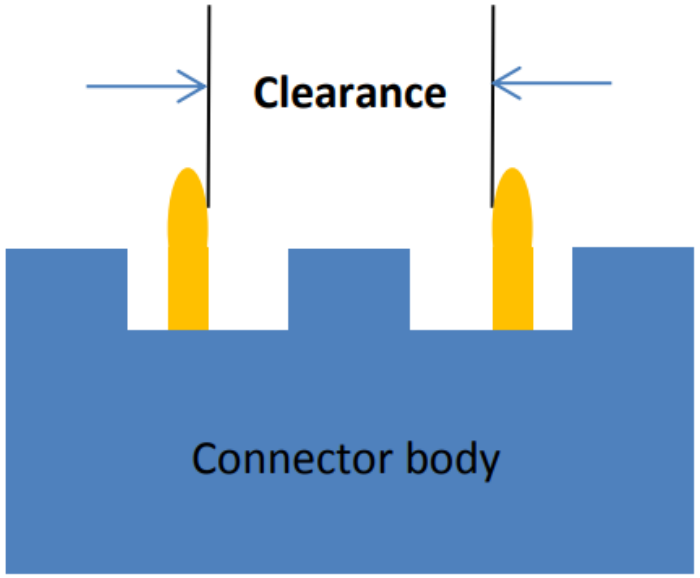
- Insulators block voltage and prevent unwanted current from flowing…
- Until they reach their limit and undergo **dielectric breakdown**
- Breakdown occurs when electric field exceeds material's dielectric strength

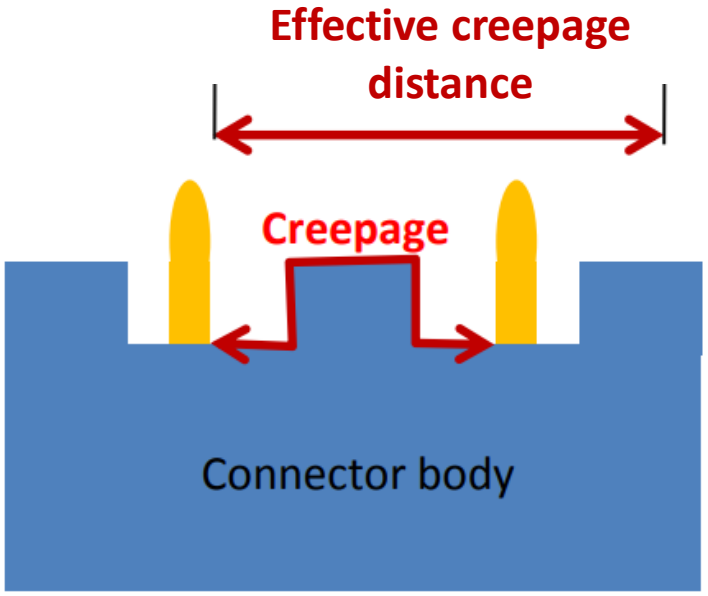
Common PCB Insulators	Dielectric Strength (kV/mm)
Air	3
FR4	20
Solder mask	> 20
Kapton (polyimide) tape	300

Uncommon PCB Insulators	Dielectric Strength (kV/mm)
Diamond	2000

Add space around high-voltage nets to avoid breakdown

- Two types of spacing requirements: clearance and creepage
- **Clearance** is distance “in air” between two nets
- **Creepage** is shortest distance along insulating surface (e.g. the PCB)

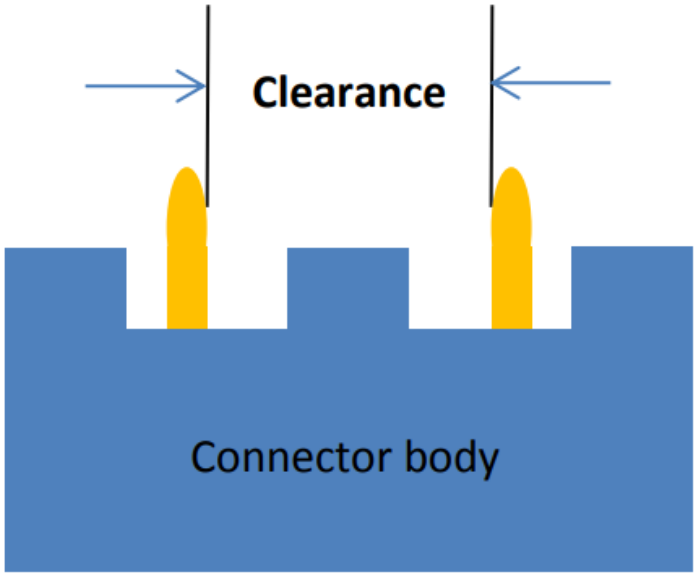




https://blog.samtec.com/wp-content/uploads/2019/04/Clearance-and-Creepage-Dave-Scopelliti.pdf

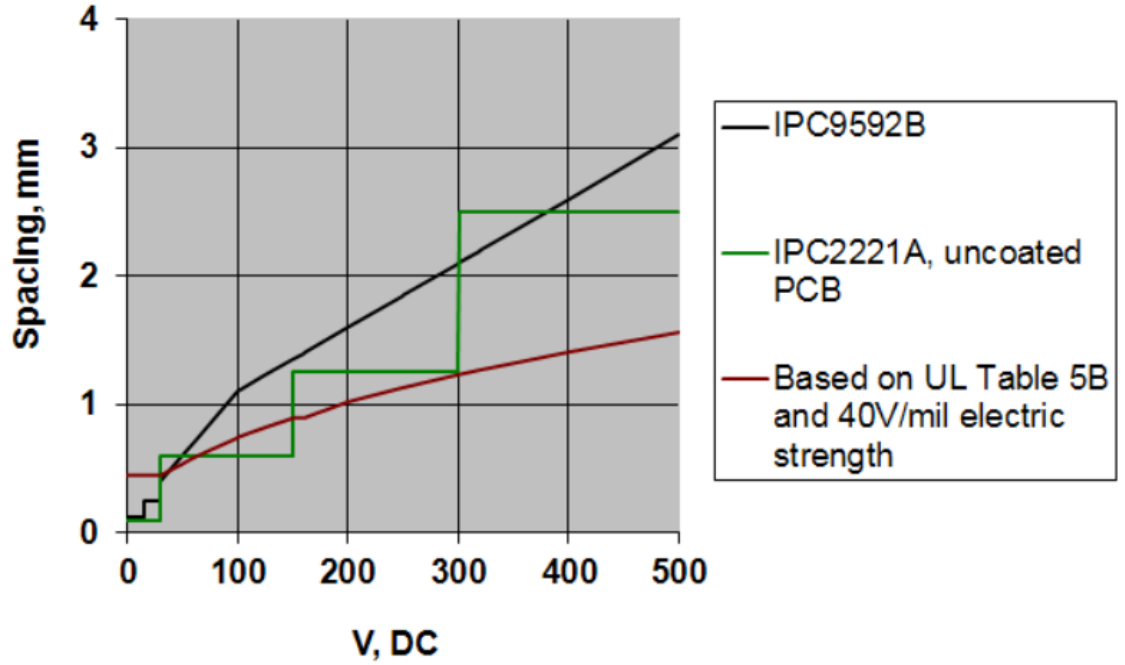
Clearance

- Refers to space in air between two exposed nets
- In PCB design rules, also refers to spacing between two conductors (even if they’re covered in an insulator)



Clearance Standards

- Standards (e.g. IPC 2221) provide PCB spacing requirements
- Various calculator tools to compute required spacing (links below)

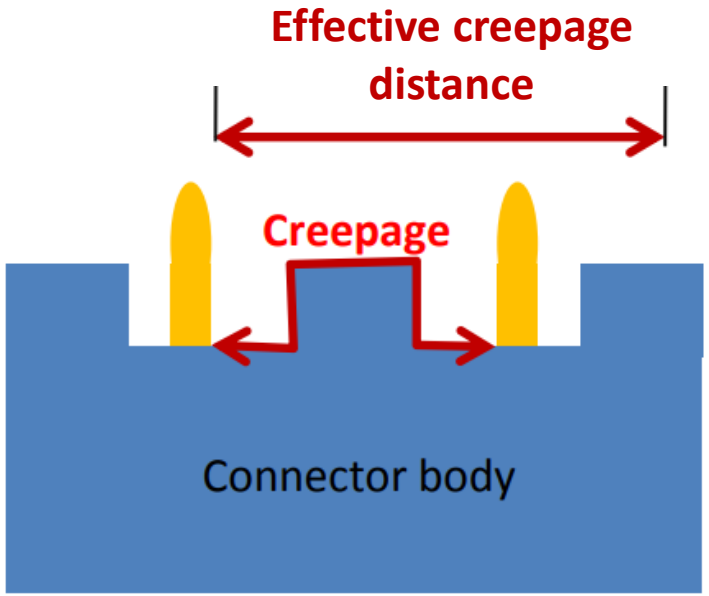


Different standards give (dramatically) different guidelines

https://resources.altium.com/p/using-an-ipc-2221-calculator-for-high-voltage-design
https://saturnpcb.com/saturn-pcb-toolkit/

Creepage

- Distance on surface between two nets
- If surface becomes “polluted,” its resistance can decrease, making it easier for electrical breakdown to occur
- Types of pollution:
  - Environmental (from exposure to the elements)
  - Carbonization (from circuit operation)



Environmental Pollution Classes

Classes	Descriptions	Examples
Pollution degree 1	• There is no pollution or only dry, nonconductive pollution	• **Sealed** components (coated PCB), clean room
Pollution degree 2	• Temporarily becomes conductive because of occasional condensation	• Telecom enclosure by IEC 60950-1 or IEC 62368-1 • Lab, office
Pollution degree 3	• Subject to conductive pollution • Nonconductive pollution that could become conductive **from expected condensation**	• Industrial, unheated factory rooms and farming
Pollution degree 4	• Continuous conductivity occurs because of conductive dust, rain or other wet conditions	• Outdoor applications

https://www.ti.com/lit/ml/slup421/slup421.pdf?ts=1768806046330

Example Creepage Table

Creepage requirements increase with…

pollution degree

voltage

RMS Voltage (V)	PCBA CREEPAGE DISTANCE TABLE (Minimum Distances – mm)								
	Pollution Degree								
	1	2	1	2			3		
	Material Group								
	Printed Boards		Other Materials						
	I, II, IIIa, IIIb	I, II, IIIa	I, II, IIIa, IIIb	I	II	IIIa, IIIb	I	II	IIIa, IIIb
25	0.025	0.04	0.125	0.5	0.5	0.5	1.25	1.25	1.25
32	0.025	0.04	0.14	0.53	0.53	0.53	1.3	1.3	1.3
40	0.025	0.04	0.16	0.56	0.8	1.1	1.4	1.6	1.8
50	0.025	0.04	0.18	0.6	0.85	1.2	1.5	1.7	1.9
63	0.04	0.063	0.2	0.63	0.9	1.25	1.6	1.8	2.0
80	0.063	0.1	0.22	0.67	0.95	1.3	1.7	1.9	2.1
100	0.1	0.16	0.25	0.71	1.0	1.4	1.8	2.0	2.2

https://www.ema-eda.com/ema-resources/blog/pcb-clearance-and-creepage-distance-table/

Board carbonization

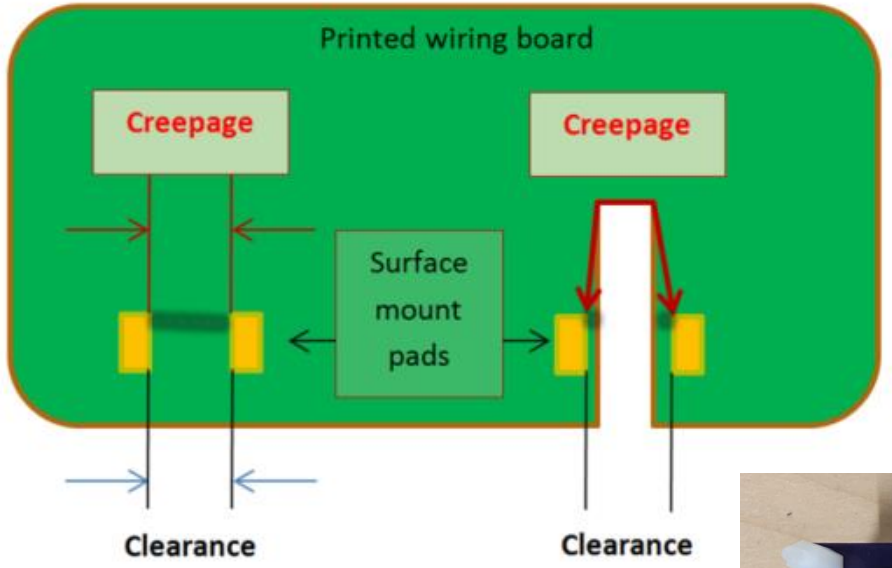
- **Carbonization** is the formation of a conductive layer of carbon on PCB when it is burnt
- **Tracking** is when unwanted current flows along carbonized paths
- Two mechanisms of carbonization to consider:

Full discharge (not enough clearance)

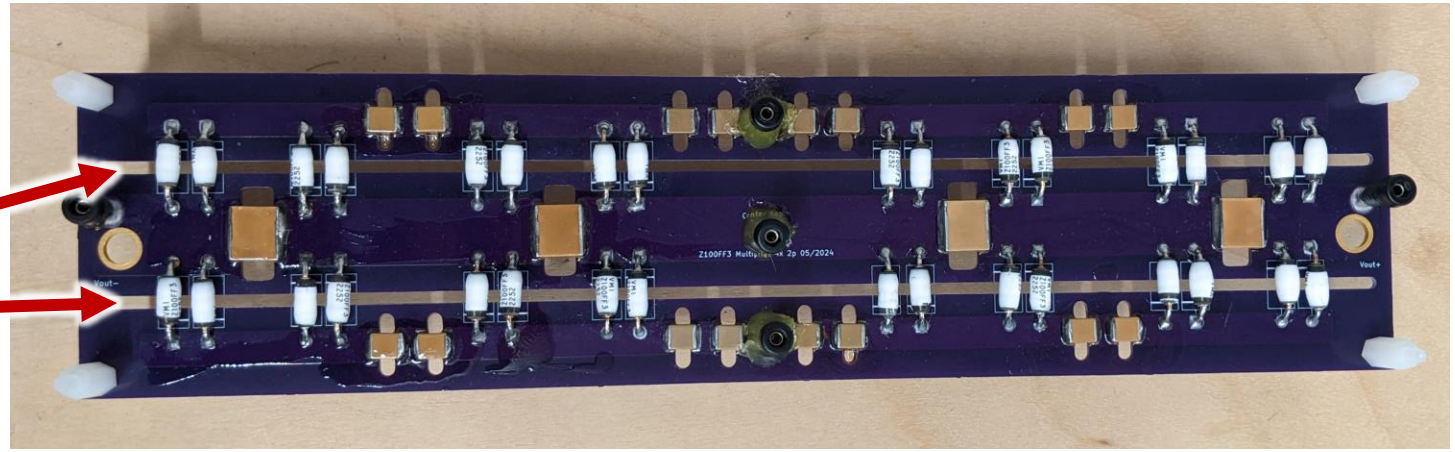
Partial discharge (corona)

https://blog.samtec.com/wp-content/uploads/2019/04/Clearance-and-Creepage-Dave-Scopelliti.pdf

Minimizing tracking: board cutouts



Board cutouts increase creepage

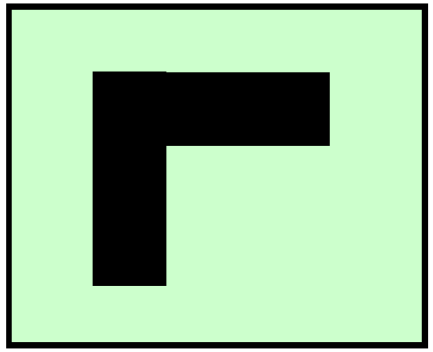


Mihir Shevgaonkar, Voltage Multiplier Rectifier, MIT 2024

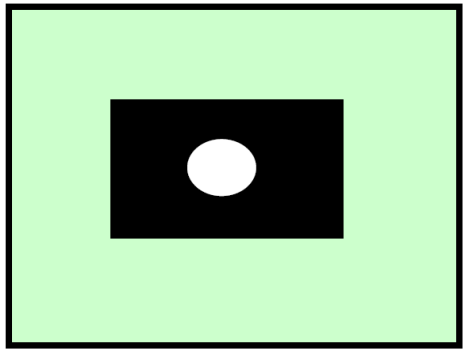
https://blog.samtec.com/wp-content/uploads/2019/04/Clearance-and-Creepage-Dave-Scopelliti.pdf

Minimizing corona: avoid sharp corners

- Sharp corners concentrate electric field, causing corona

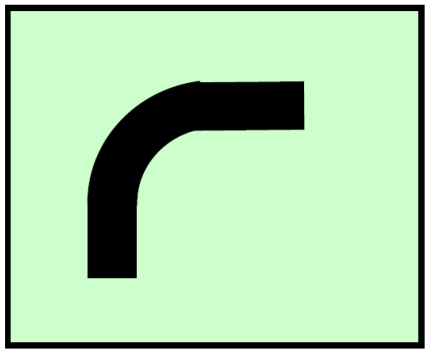


Bad corner design

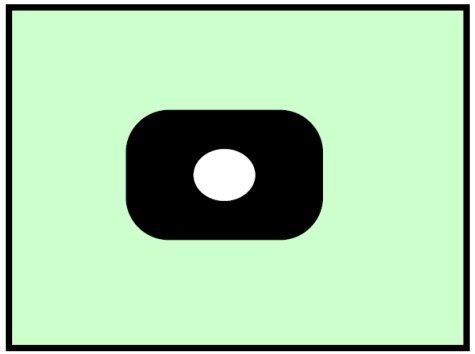


Bad pad design

- Instead, choose rounded traces and pads



Good corner design



Good pad design

Other manufacturing techniques

Conformal coating

Potting

https://www.hanastglue.com/products/potting-adhesive/1-1-Silicone-potting-compound/hn-8806-hdsxjg.html

High-Current Considerations

High current causes temperature rise

$$R = \frac{\rho L}{A}$$

Everything has resistance (even copper)!

$$P_{\text{diss}} = I^2 R$$

Power dissipated in resistance

$$\Delta T = P_{\text{diss}} R_{\text{th}}$$

Temperature rise due to power dissipated

Thermal resistance (°C/W)

What is thermal resistance?

- Linearly relates temperature rise to dissipated power

$$\Delta T = P_{\text{diss}} R_{\text{th}}$$

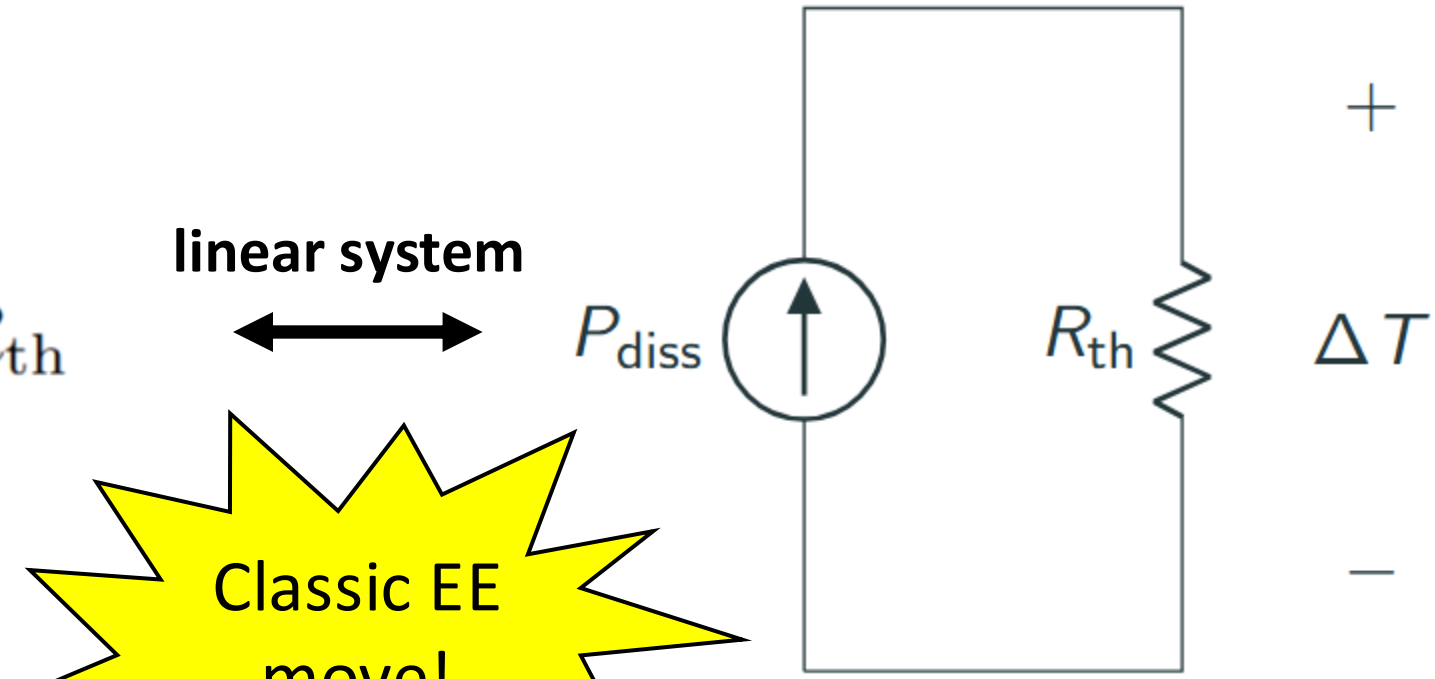
- Units: °C/W
- Given by manufacturer
- Part of a “thermal circuit” model

Thermal Circuit Model

- Acts like electrical circuit model, but represents thermal behavior

$$\Delta T = P_{\text{diss}} R_{\text{th}}$$

linear system



Classic EE move!

How can we use this thermal model?

- Calculate minimum size for traces and vias
- Calculate temperature rise in components
  - Choose an appropriate component
  - Figure out how to cool it

Choose trace size based on current

To decrease resistance…

$$R = \frac{\rho L}{A}$$

Increase conductor cross-sectional area

Increase area by:

- Increasing trace width (layout)
- Increasing copper thickness (manufacturing)

$$P_{\text{diss}} = I^2 R$$

$$\Delta T = P_{\text{diss}} R_{\text{th}}$$

Trace width example

- Given:
  - 10 A current
  - 20°C temperature rise
- Calculate: 250 sq. mil area
  - 1 oz/ft^2 copper: 200mil trace width
  - 2 oz/ft^2 copper: 100mil trace width
- Internal traces require more area since they don't dissipate heat as easily

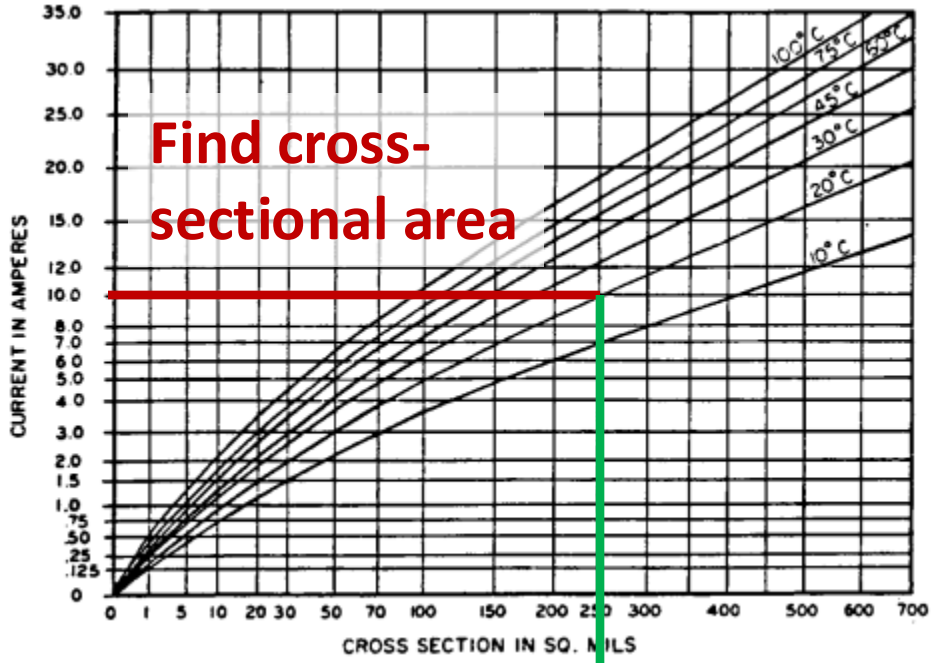


Figure A External Conductors

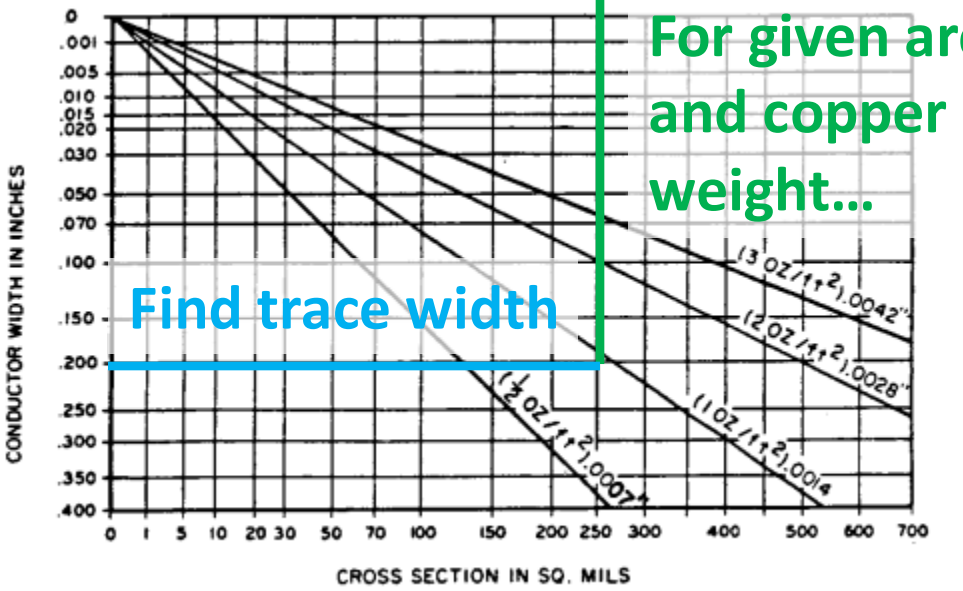
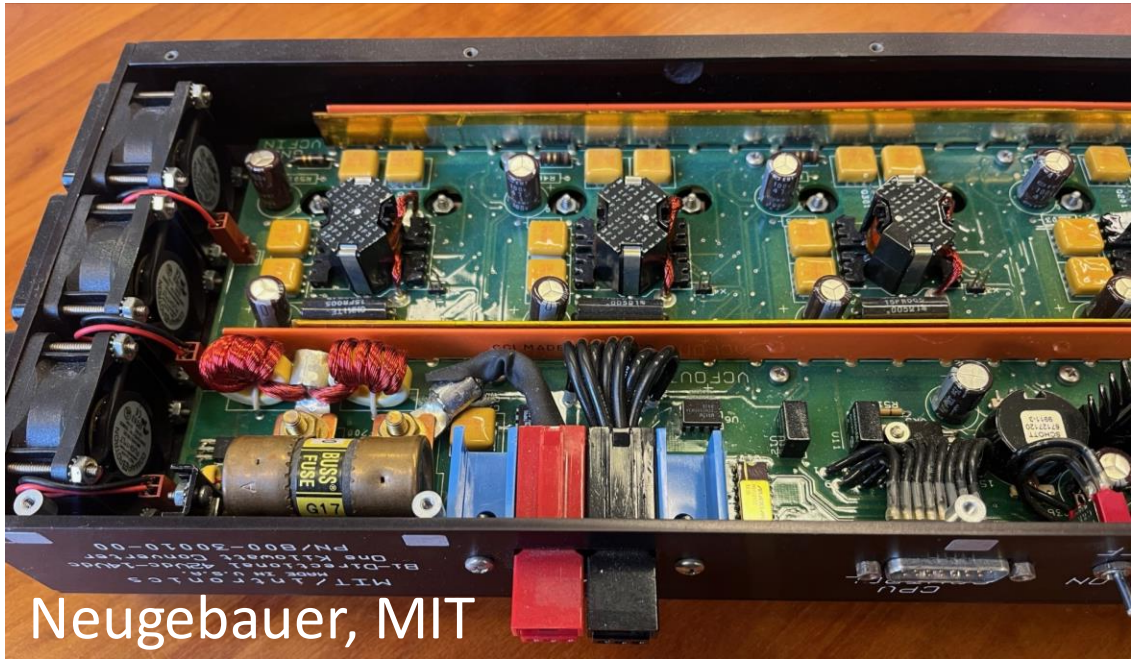


Figure B Conductor width to cross-section relationship

https://www-eng.lbl.gov/~shuman/NEXT/CURRENT_DESIGN/TP/MATERIALS/IPC-2221A(L).pdf

What if we want even more conductor area?

- Ultra-thick copper (10oz, 20oz)
- Copper busbars
- Mounted wires



Neugebauer, MIT

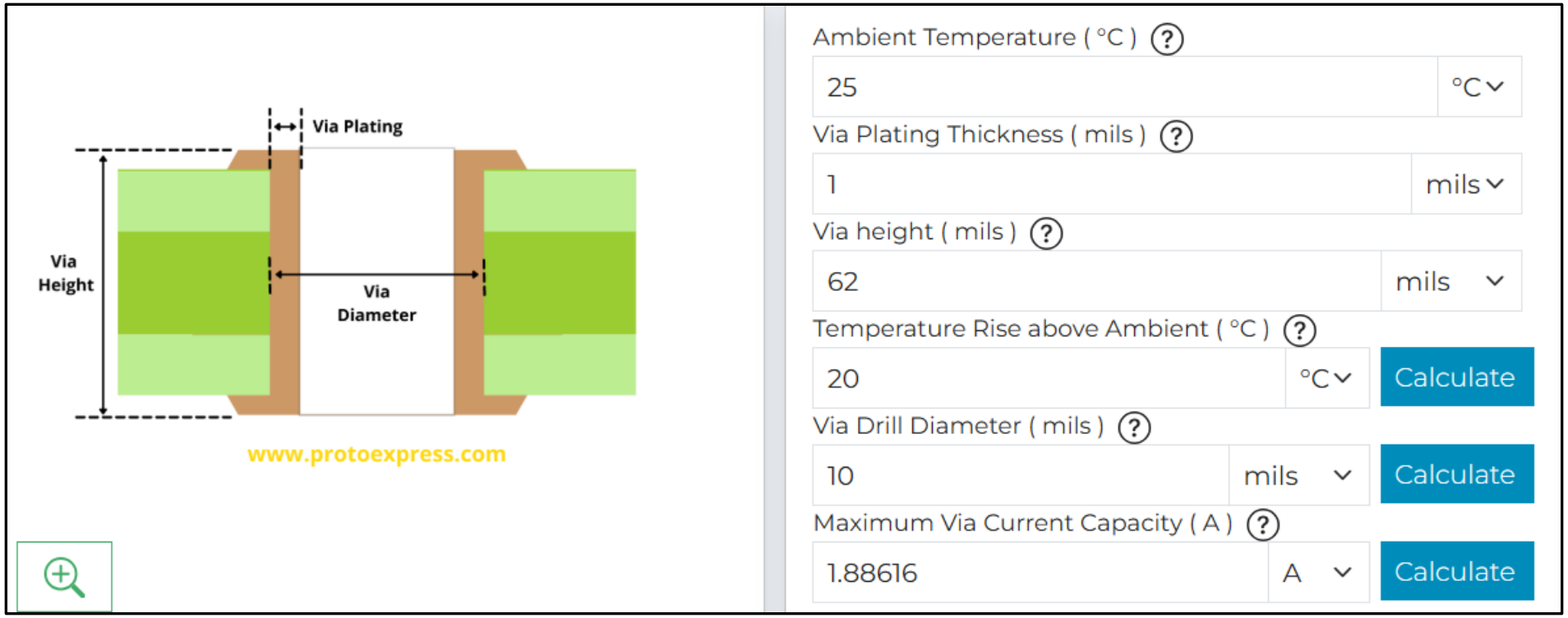
AC current considerations

- Previous slides considered dc/low-frequency current
- At higher frequencies, current is not distributed evenly throughout conductor due to “skin effect”
- Current effectively only flows within one “skin depth” of surface, so loss increases with frequency

$$\text{Skin depth } \delta = \sqrt{\frac{\rho_{\text{Cu}}}{\pi \mu_{\text{Cu}} f}} = \frac{K}{\sqrt{f}}$$

Vias for high-current paths

- Use parallel vias to get a high-current trace to another layer
- Calculators give each via's current-carrying capacity



Protoexpress Designer Tools

Transistor selection example

- Suppose we want a transistor that can handle 150 V, 4 A, 60°C rise
- Try Fairchild FQPF7N20L: 200 V, 5 A leaves some margin

FAIRCHILD SEMICONDUCTOR™

December 2000

QFET™

FQPF7N20L

200V LOGIC N-Channel MOSFET

G D S

TO-220F

FQPF Series

General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary,

Features

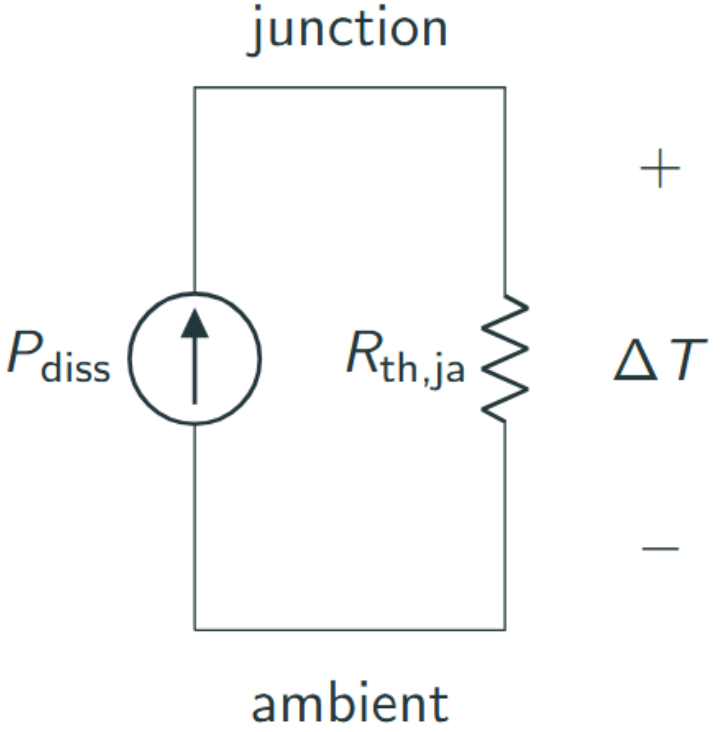
- 5.0A, 200V, $R_{DS(on)}$ = 0.75Ω @V_{GS} = 10 V
- Low gate charge (typical 6.8 nC)

Attempt 1: No heat sink

- No heat sink: use junction-to-ambient thermal resistance

$$P_{\text{diss}} = I^2 R_{\text{ds,on}} = 12\,\text{W}$$

$$\Delta T = P_{\text{diss}} R_{\text{th,ja}} = 744\,^\circ\text{C}$$



Thermal Characteristics

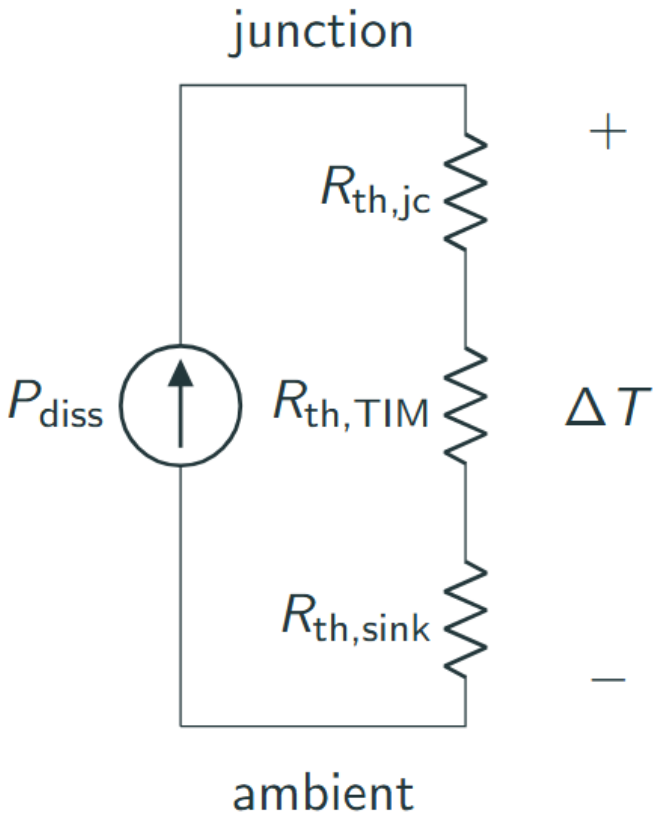
Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	3.38	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	°C/W

Attempt 2: Add a basic heat sink

V7236B1

DigiKey Part Number	A10756-ND
Manufacturer	Assmann WSW Components
Manufacturer Product Number	V7236B1
Description	HEATSINK TO-220 19.05X13.21MM
Manufacturer Standard Lead Time	17 Weeks

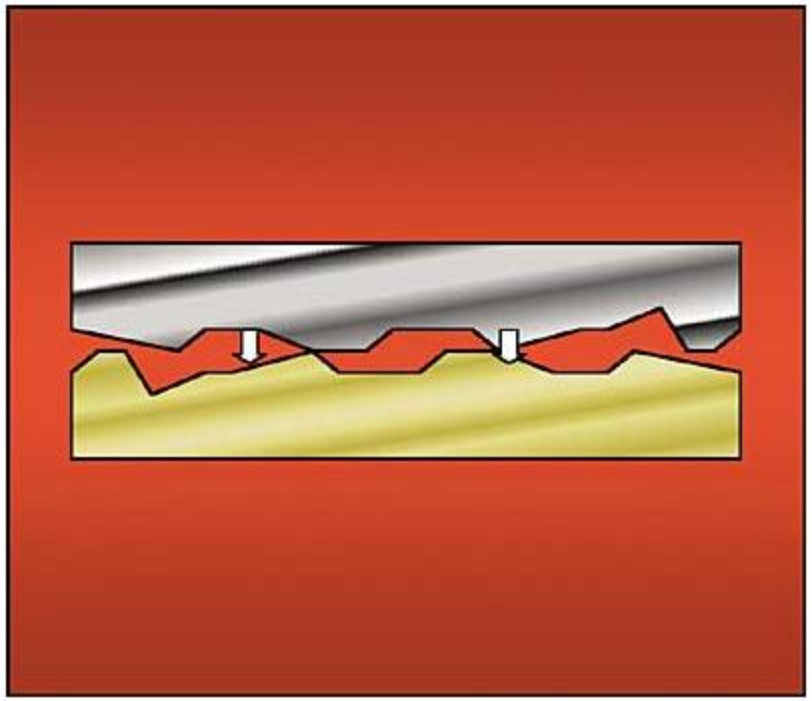
$$R_{\text{th,sink}} = 24\,^{\circ}\text{C/W}$$



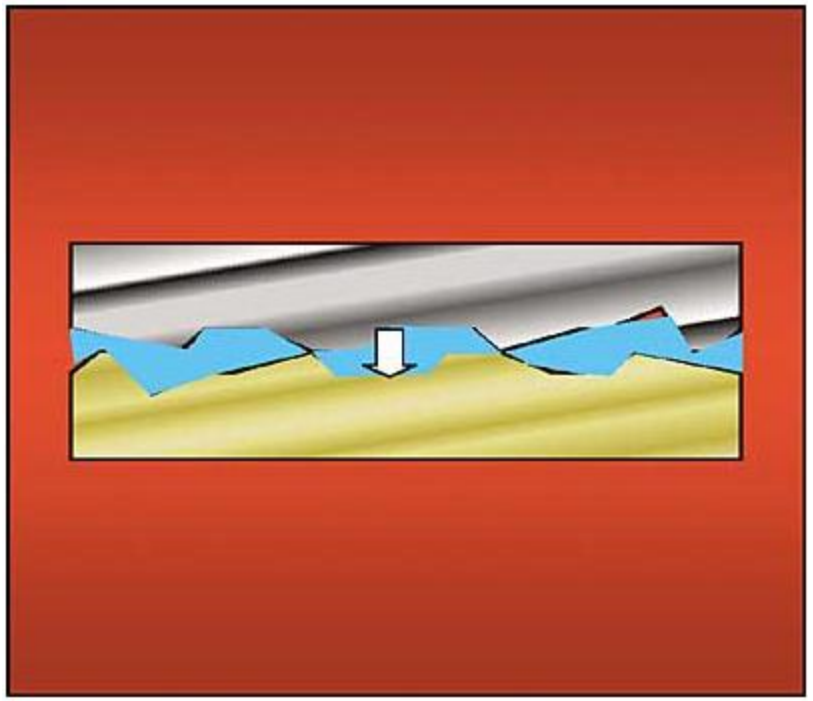
Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	3.38	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	°C/W

Aside: Thermal interface material



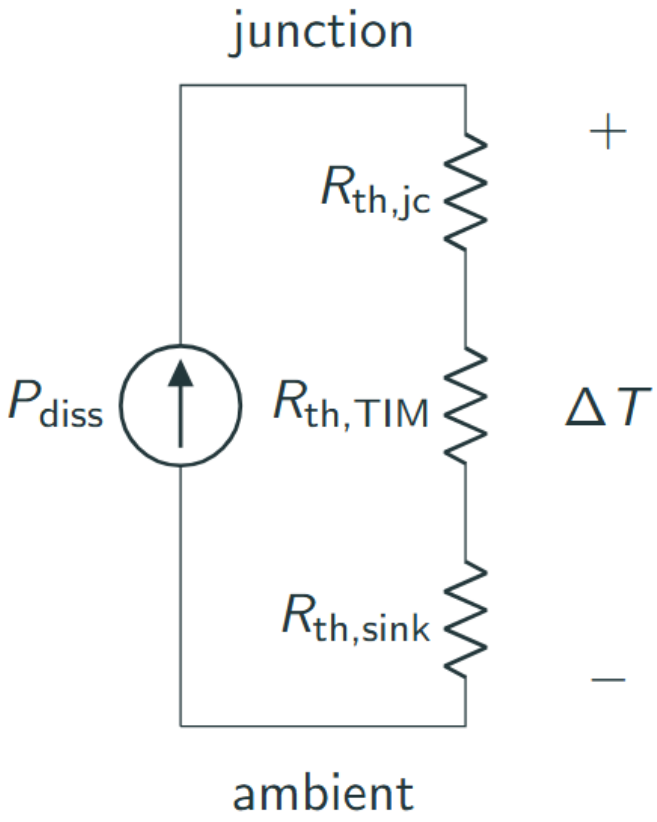
Metal-to-metal interface (transistor to heat sink) doesn't make good contact



Add thermal interface material to fill the gaps

Attempt 2: Add a basic heat sink

$$R_{\mathrm{th,jc}} = 3.38\,^{\circ}\mathrm{C/W}$$
$$R_{\mathrm{th,TIM}} = 0.02\,^{\circ}\mathrm{C/W}$$
$$R_{\mathrm{th,sink}} = 24\,^{\circ}\mathrm{C/W}$$
$$\overline{R_{\mathrm{th,tot}} = 27.4\,^{\circ}\mathrm{C/W}}$$



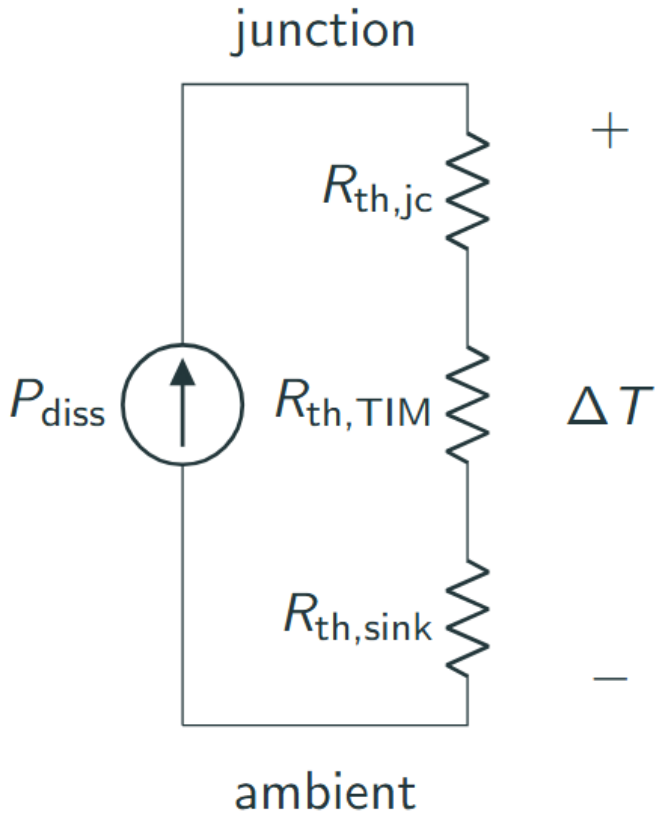
$$\Delta T = P_{\mathrm{diss}} R_{\mathrm{th,tot}} = 329\,^{\circ}\mathrm{C}$$

Attempt 3: What size heat sink do we need?

$$R_{\mathrm{th,sink}} \leq \frac{\Delta T}{P_{\mathrm{diss}}} - R_{\mathrm{th,jc}} - R_{\mathrm{th,TIM}}$$

$$R_{\mathrm{th,sink}} \leq 1.6\,^{\circ}\mathrm{C/W}$$

That's a really big heat sink!

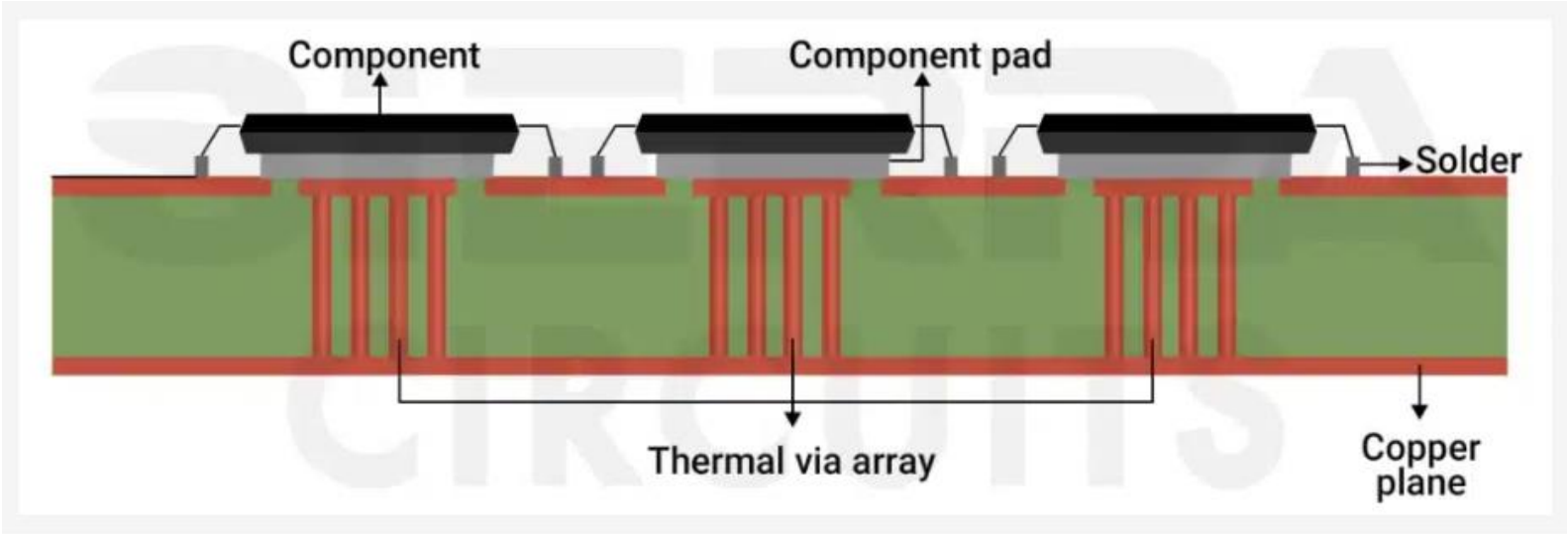


Transistor selection takeaways

- Often, datasheet current ratings assume an unrealistic cooling scenario
- Choose bigger transistor!
- Other ways you can decrease thermal resistance:
  - Increase heat sink size
  - Extra copper area on PCB
  - Forced-air cooling (fan)
  - Liquid cooling

Thermal vias

- Conduct heat to other side of the board
  - 10mil via from previous example: 180 °C/W
  - May need many vias!
- Bottom-side-cooled packages: heat sink on other side of board



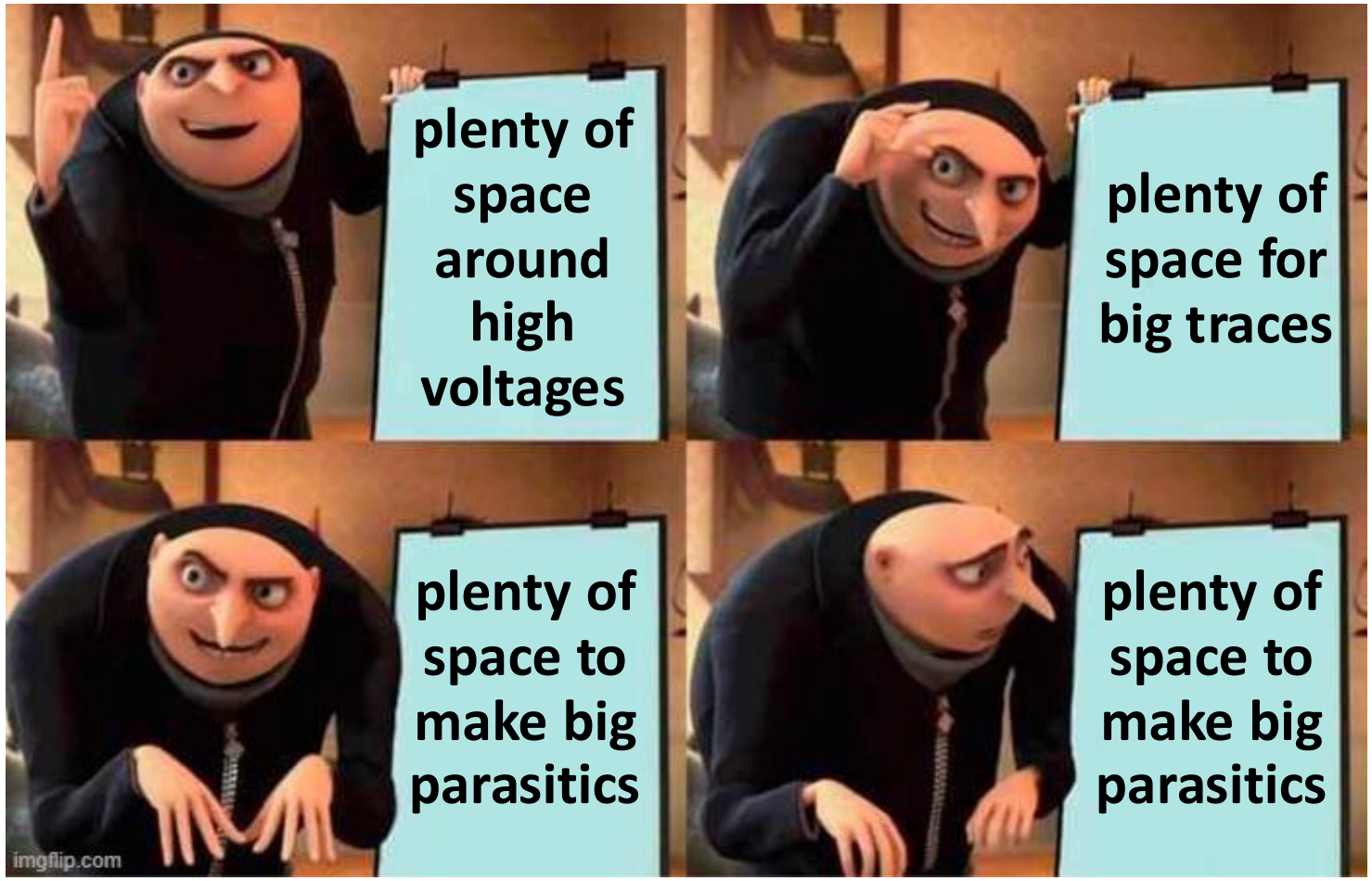
https://www.protoexpress.com/kb/how-thermal-vias-enhance-heat-dissipation-in-pcbs/

Quick review

- High voltage: add more space
- High current: make conductors bigger

"I'll just make my whole board really big!"

What if we make the whole board big?



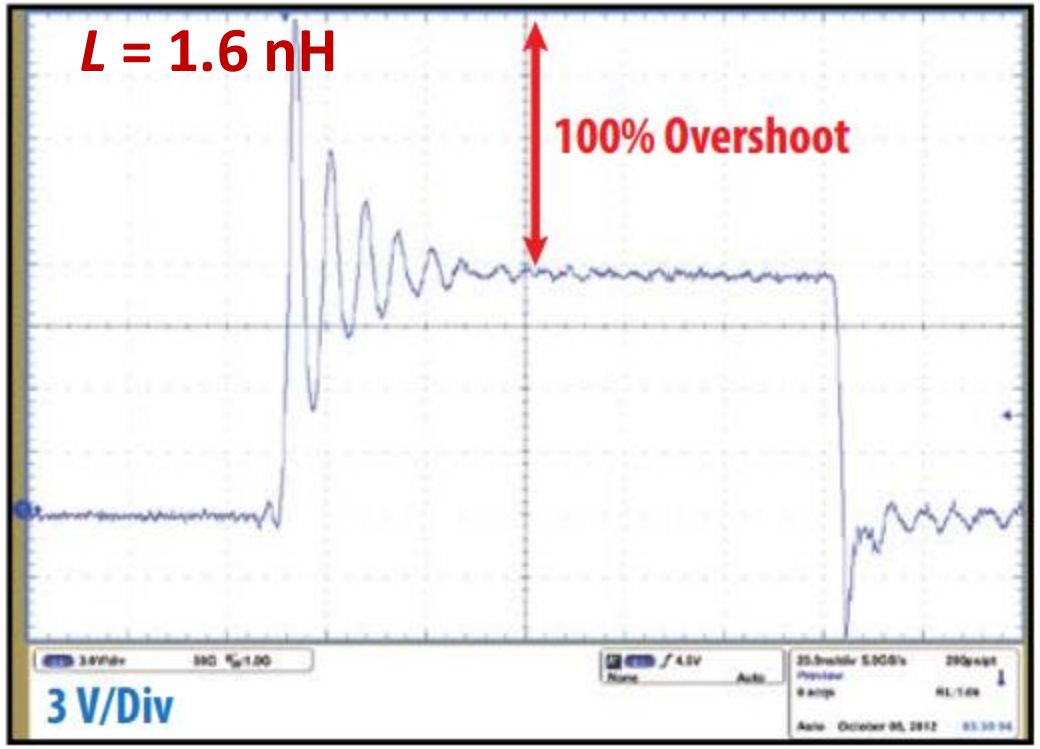
Parasitic inductance

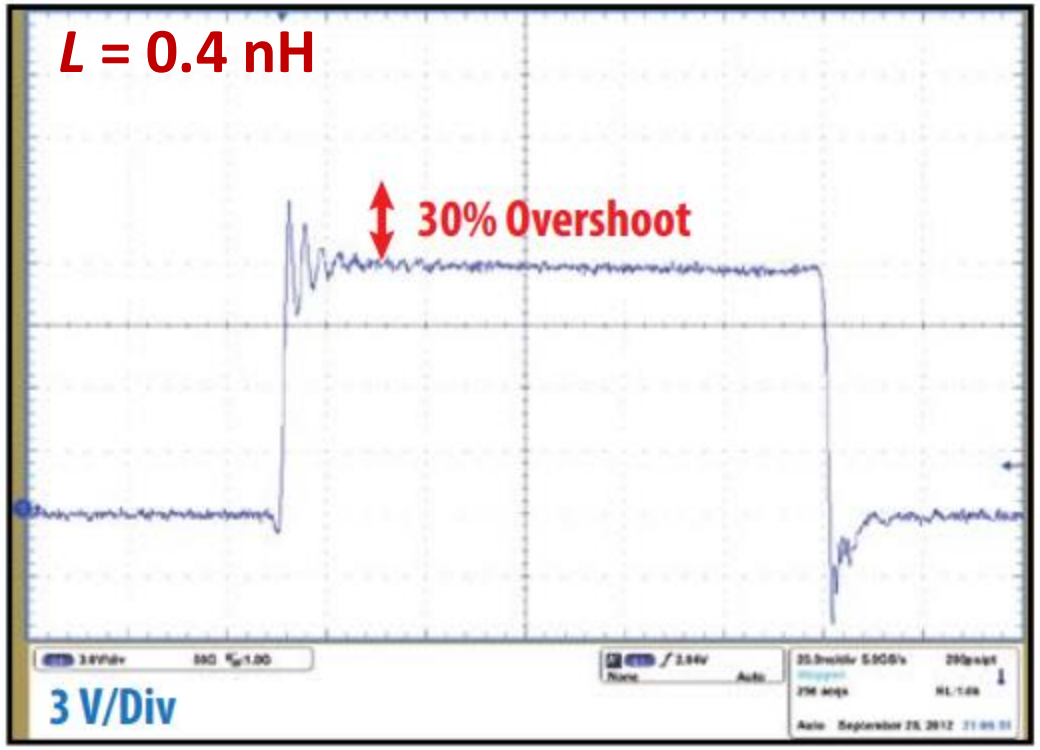
$$v_L = L\frac{\mathrm{d}i_L}{\mathrm{d}t}$$

- If di/dt is high, parasitic inductance will see a high transient voltage
- KVL means that something else (e.g. a switch) will also see this unwanted transient voltage

Parasitic inductance

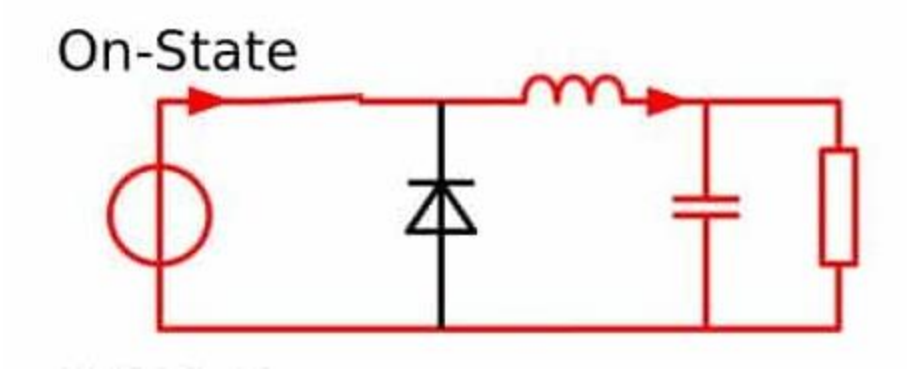
- Oscillates with circuit's capacitance, creating noisy ringing





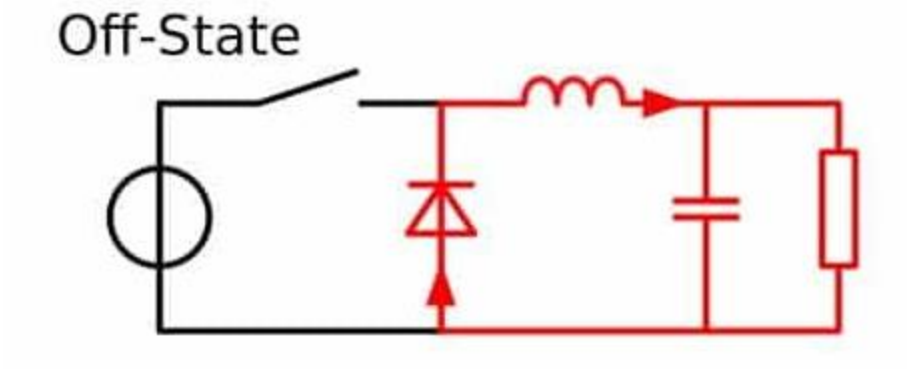
https://epc-co.com/epc/Portals/0/epc/documents/papers/optimizing%20pcb%20layout%20with%20egan%20fets.pdf

Switching induces high di/dt



Top switch conducts all current

High di/dt during switching transitions!



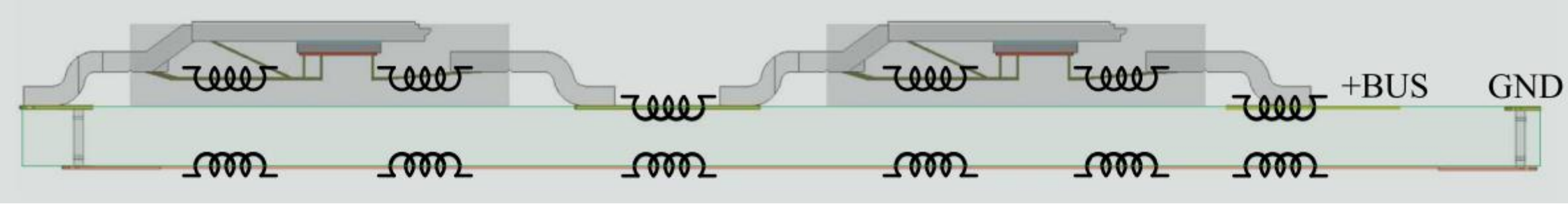
Top switch conducts no current

Reducing parasitic inductance

- Inductance is larger when **loop area** is larger
  - More space to link magnetic flux!
- Want to minimize space between current and its return path

Example 1: Large loop area

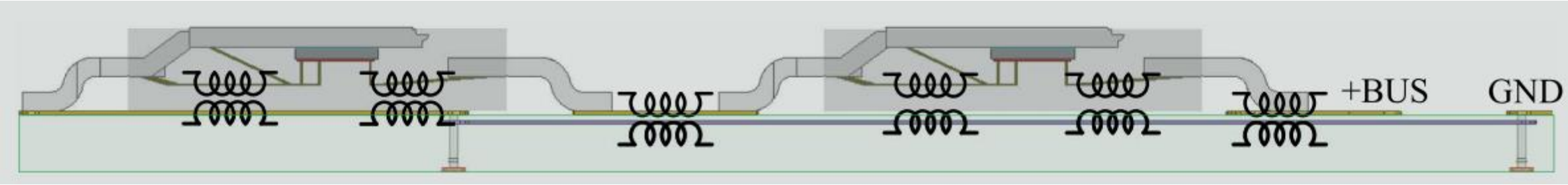
- Components on top layer, return path on bottom layer
- Loop area includes full thickness of board
- Large parasitic inductance :(



E. Persson, “Optimizing PCB Layout for HV GaN Power Transistors,” IEEE Power Electronics Magazine, June 2023.

Example 2: Small loop area

- Components on top layer, return path on layer 2
- Loop area does **not** include full thickness of board
- Small parasitic inductance :)



E. Persson, “Optimizing PCB Layout for HV GaN Power Transistors,” IEEE Power Electronics Magazine, June 2023.

Parasitic capacitance

- Can introduce noise
- Want to minimize at high-frequency, high-voltage nodes

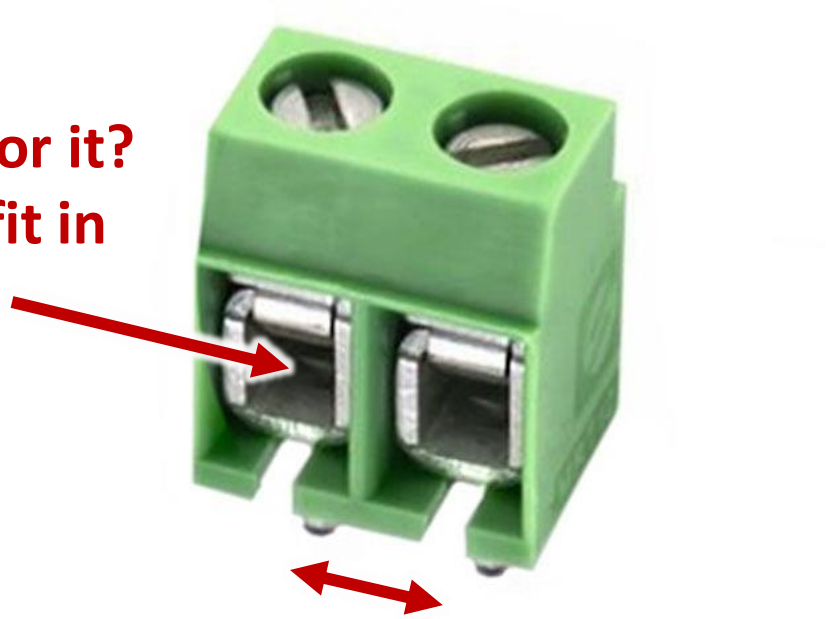
Keep conductor area small!

$$C = \frac{\epsilon A}{d}$$

Other Practical Considerations

High-power connectors

Current: is connector rated for it? And can chosen wire gauge fit in holes?



Voltage: is connector rated for it? (i.e. are terminals far enough apart?)

High-power connectors

Wire to board
Screw wires in directly
Must unscrew every time you move the board :(

Plug and socket
Two pieces that connect
Easy to plug and unplug! :)

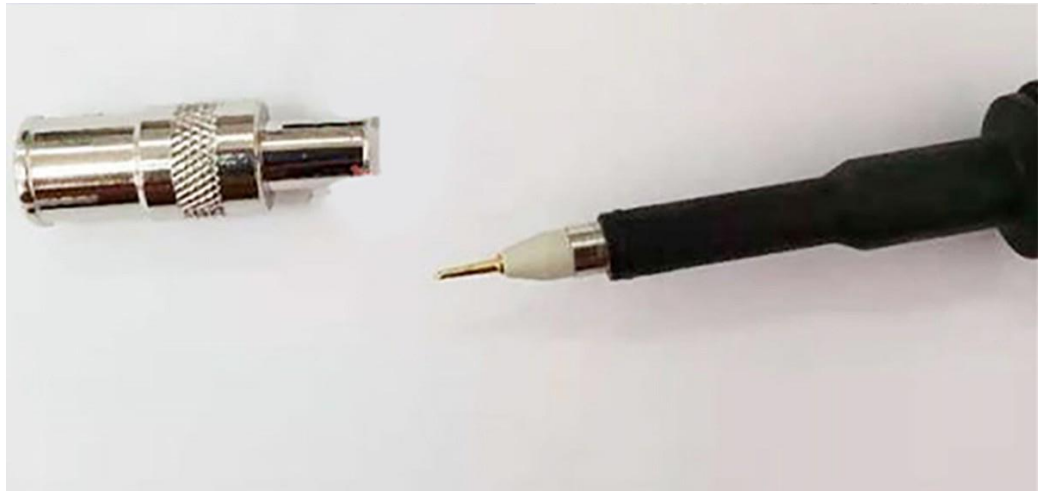
Test points must be hands-off

Rings

- Clip a probe on
- Separate ground lead

Coaxial

- Stick probe in
- No ground lead



Conclusions

- Ensure sufficient space around high-voltage nets
- Ensure sufficient conductor area for high currents
- Build thermal circuit models for high-current components
- Minimize parasitic inductance and capacitance
- Consider practical testing needs in board design